A Switched-Current Sample-and-Hold Amplifier for FM Demodulation

by

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A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Department of Electrical and Computer Engineering
University of Toronto

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A Switched-Current Sample-and-Hold Amplifier for FM Demodulation

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Degree of Master of Applied Science
1995

Abstract

A switched-current sample-and-hold circuit is designed. The circuit is fabricated in a 0.8μm BiCMOS process, the operation of the circuit is analyzed and is supported by simulation. Measurement indicates a sampling frequency of 57 MHz with 10 bits linearity and suggests that operation at sampling frequencies beyond 80 MHz is feasible. Comparison of this circuit with some other switched-current sample-and-hold circuits is given to highlight the strengths and weaknesses of this circuit. The functionality of the sample-and-hold circuit as a under-sampler in the CT2PLUS personal communication system is also verified.

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And, to Christopher Neufeld, thank you for everything you have done for me, and for always being there.

Table of Contents

CHAPTER 1 Introduction

This thesis deals with the design and implementation of a current-mode sample-and-hold circuit. Several perspectives, including trade-offs between speed and accuracy, implementation of switches, and methods of reducing charge-injection errors are discussed. The circuit is fabricated in Northern Telecom's 0.8μm BiCMOS process.

One application of the circuit is in the CT2Plus personal communication system. Such wireless communication applications often require battery operation; therefore, power consumption is a major concern. Various architectures of sample-and-hold systems are explored with the aim of achieving both high-speed and high-accuracy performance maintaining low power consumption. HSPICE [1] simulation is used to study the design, and experimental work is done to verify the real-time performance of the circuit.

1.1 Thesis Motivation

The demand for portable equipment such as cellular phones, digital cordless phones, and wireless LANs has grown rapidly in recent years. These systems often employ digital signal processing because this can result in a high performance system with a small size, low cost, and compatibility with digitally-coded transmissions.

However, due to the fact that the vast majority of signals in the world around us are analog, analog mixing stages and analog-to-digital converters are often needed between the antenna and the digital circuitry. In many data conversion systems, a sample-and-hold circuit is required to hold the analog signal for certain period of time so that the A/D converter can perform the conversion. Quite often, the performance of the sample-and-hold circuit puts a limit on the maximum achievable speed and accuracy of the overall data-conversion system. Therefore, there is an interest in designing a high-speed and high-accuracy sample-and-hold circuit with low-voltage operation and low-power consumption.

Specifications to guide the work in this thesis are obtained from Communications Canada and Bell-Northern Research [2][3][4]. Document RSS-130 from Communications Canada describes the radio standard specification for digital cordless telephones in the band 944 to 948.5 MHz. One possible receiver architecture was proposed by Bell-Northern Research. Two key components in the receiver are a sample-and-hold circuit and a limiting amplifier. The specification for the system indicates that the sample-and-hold circuit takes an input signal centered at 150.048 MHz with a 100 kHz bandwidth. A sampling frequency of 1.152 MHz is utilized. Low aperture jitter is needed for the sample-and-hold circuit so that it does not introduce phase noise into the signal. For this reason and also to ensure a fast settling time in the sample-mode, the sampling-rate for the design is set to be 50 MHz. The noise figure of the sample-and-hold circuit should be less than 2 dB. 8-bits accuracy is required for the sample-and-hold circuit, and the circuit should draw less than 25 mW at a supply voltage of 3 to 5V in the base station. In the portable handsets, the power consumption should be less than 10 mW at 2.8 to 3V. A detailed description of the CT2Plus system and the specification to guide the work in this thesis is in Chapter 2.

1.2 Thesis Outline

The design and application of a current-mode sample-and-hold circuit with low power consumption is the main focus of this thesis.

This thesis is divided into six chapters. Chapter 2 gives an introduction to the CT2Plus personal communication system where the sample-and-hold circuit designed is to find an application. This explains the motivation and sets the guidelines for the work in this thesis. Chapter 3 gives the background information on various architectures for sample-and-hold systems. Trade-offs between speed and accuracy are discussed, and a comparison between voltage-mode and current-mode design is presented. Different ways to implement switches are also discussed. In chapter 4, an appropriate architecture for the sample-and-hold circuit is chosen and circuits are designed for it. Simulations are used to check the performance of the circuit, and the results are presented. The circuit was fabricated in $0.8\mu m$-BiCMOS process, and test related issues are presented in Chapter 5. The functionality of the sample and-hold circuit as a decimator in the CT2Plus system is also verified. Testing results are summarized. Chapter 6 contains the conclusion of the work in this dissertation and issues related to future work.

CHAPTER 2 Application

The sample-and-hold circuit designed in this thesis has an application in the receiver of the CT2Plus personal communication radio. In this chapter, a description of the CT2Plus system is presented, and the requirements for the sample-and-hold decimator are given. This should serve to clarify the motivation and guidelines for the work in this thesis.

2.1 System Specification

In January 1993, Communications Canada released the radio standard specification for a low power Digital Cordless Telephone (DCT) operating according to the CT2Plus Class 2 Common Air Interface [2][3]. The CT2Plus equipment is to be used to convey digitally-encoded speech, with associated digital signalling via a radio frequency channel, to and from the Public Switched Telephone Network. The CT2Plus Class 2 standard is based on the European common air interface for second-generation cordless telephone (CT2) equipment [4].

The equipment specification for the Digital Cordless Telephone in the band of 944 to 948.5 MHz is listed in documents [2], [3], and [4]. The important aspects of the equipment specification include three parts: radio-frequency (RF) interface, signalling, and speech coding and transmission. Among these, the one for the radio-frequency interface is most closely related

to the work in this thesis. In particular, the work in this thesis concentrates on parts in the radio receiver. Therefore, the specification for the radio receiver is discussed in more detail in the following section.

2.2 Specification for Radio Receiver

According to the specification for the radio-frequency interface, CT2Plus equipment operates in the frequency band of 944 MHz to 948.5 MHz. The radio channels have bandwidths of 100 kHz with center frequencies at $(943.95 + 0.1 \times n)$ MHz, where n is the channel number ranging from 1 to 40. The modulation scheme employed for the radio transmitter is Binary Frequency Shift Keying (BFSK). The demodulation of the FSK signal is performed in the radio receiver.

FSK modulation is characterized by the information contained in the frequency of the signal [5]. Under BFSK modulation, a binary 1 is encoded as a frequency higher than the carrier frequency; a binary 0 is encoded as a frequency lower than the carrier frequency. A BFSK waveform is a continuous-phase constant-envelope FM waveform. A typical set of BFSK signal waveforms $s_1(t) = A\cos(2\pi(f_c - f_d)t)$ and $s_2(t) = A\cos(2\pi(f_c + f_d)t)$ are used to convey binary digits 0 and 1 respectively, where f_c is the RF carrier frequency, and f_d is the deviation.

The generation of the BFSK signals involves the use of an FM modulator with a carrier wave $A\cos(2\pi f_c t)$. The signal can be expressed as:

$$s(t) = A\cos(2\pi f_c t + 2\pi f_d \int_{-\infty}^{t} D(\alpha)d\alpha + \theta) \qquad (2.1)$$

where $D(t)$ is a binary waveform with value 1 when the binary signal is 1 and -1 when the binary signal is 0; and θ is the phase angle of the carrier signal at time $t = 0$. In this system, the nominal data rate is 72 kb/s.

For the demodulation of a binary FSK signal, a limiter and a discriminator must be used. In practice, it is difficult to implement the limiter-discriminator circuit beyond a few tens of megahertz. However, the frequency band that CT2Plus equipment works in is over 900 MHz. To

solve this problem, a double-conversion scheme is used.

2.3 Receiver Configuration

In a double-conversion receiver, the frequency of the received signal is down-converted twice before it reaches the baseband. The block diagram of a typical double-conversion receiver is shown in Fig. 2.1.

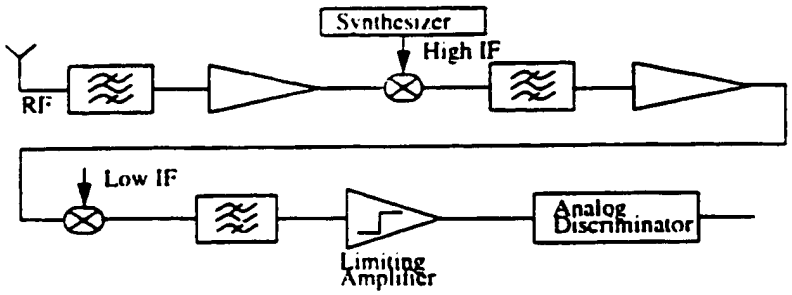


Figure 2.1 Typical double-conversion receiver

In the diagram, the IF filter is used to do most of the channel filtering and pulse shaping. The first mixer is used to bring the RF signal down to a high IF signal, and the second mixer is used to bring down the high IF signal to a low IF signal where the signal then goes through a limiting amplifier and an analog discriminator circuit.

The envisioned implementation of the receiver for the CT2Plus system, which is proposed by Bell-Northern Research (BNR) is shown in Fig. 2.2. In this configuration, the RF signal is in

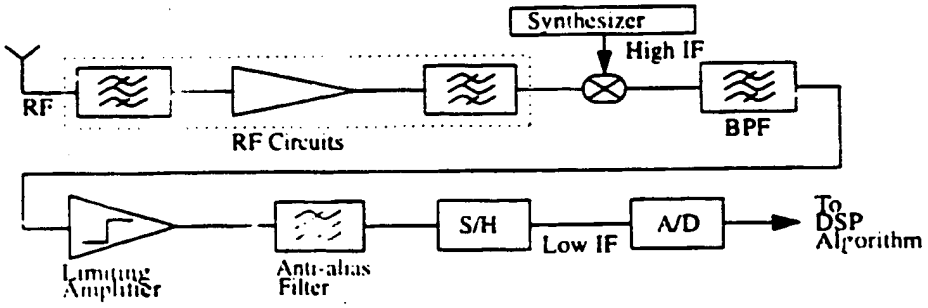


Figure 2.2 Receiver structure

frequency band of 944 MHz to 948.5MHz, the high IF signal is centered at 150.048 MHz, and the

low IF signal is centered at 288 kHz. The limiting amplifier is implemented at the high IF, and the signal is under-sampled. Aliasing is used to accomplish the second down-conversion, and the resulting signal is then digitized at a relatively low rate.

The operation of the receiver can be best explained by viewing the spectrum of signals at various points in the receiver (Fig. 2.3). The need for an anti-aliasing filter and the details of using aliasing to accomplish the second down-conversion are also explained.

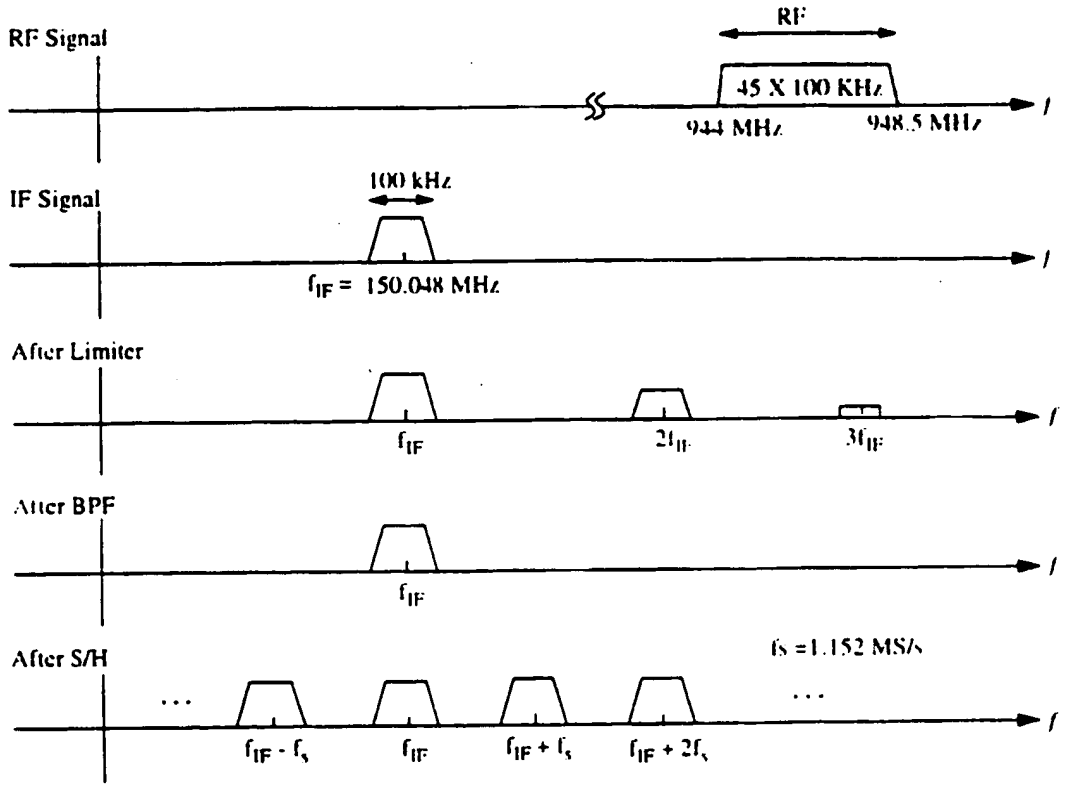


Figure 2.3 Spectrum of signals at various points in the receiver

The RF signal occupies the frequency band of 944 MHz to 948.5 MHz, which contains 45 channels each with a bandwidth of 100 kHz. After the first mixer, the RF signal is brought down to a high IF signal centered at 150.048 MHz with bandwidth of 100 kHz. This signal then goes through a limiting amplifier where the signal strength is limited.

After the limiting amplifier, harmonic distortion at frequencies nf_{IF} where n is an integer

starting from 2, and f_{IF} is the high intermediate frequency 150.048 MHz, are introduced to the signal due to gross nonlinearity of the limiter. An anti-aliasing band-pass filter, with center frequency of 150.048 MHz, is needed to filter out these harmonics.

The filtered signal is then under-sampled in the sample-and-hold amplifier at a sampling rate of 1.152 MHz. According to the Uniform Sampling Theorem for Bandpass Signals [6], a bandpass signal $x(t)$ with a spectrum of bandwidth B_x and upper frequency limit f_{xu} can be represented by instantaneous values $x(kT_s)$ if the sampling rate f_s is $\frac{2f_{xu}}{m}$ or larger, where m is the largest integer not exceeding $\frac{f_{xu}}{B_x}$. In this case, the sampling rate f_s is chosen to be 1.152 MHz. Some simple calculation shows that the sampling operation leaves the signal intact, merely repeating itself periodically at frequencies $(150.048 \pm n \times 1.152)$ MHz, where n is an integer. The 130th harmonic, which centers at 288 kHz, is then passed to the analog-to-digital convertor. As a result, the high IF signal centered at 150.048 MHz is down-converted to the low IF signal centered at 288 kHz.

After the analog-to-digital converter, the signal goes through a DSP discriminator where the demodulation of the signal is done. The simple algorithm used to demodulate the received signal is illustrated in the block diagram of the DSP quadrature demodulator and discriminator (Fig. 2.4).

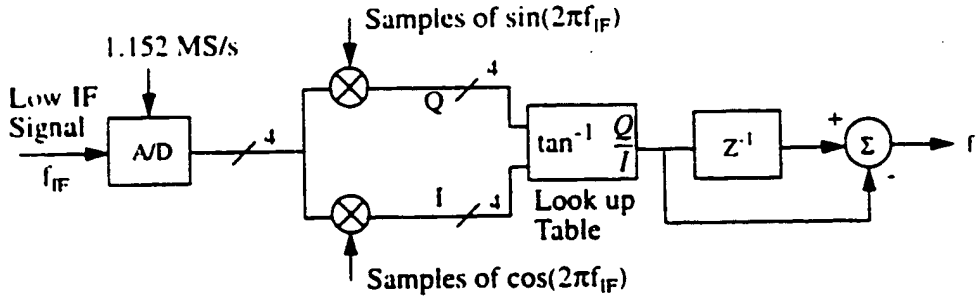


Figure 2.4 DSP quadrature demodulator and discriminator

In the analog-to-digital converter, the low IF signal is digitized and then digitally mixed to the

baseband I and Q components. The look-up table for $\text{atan}\frac{Q}{I}$ gives the phase $\varphi(n)$ of the modulated signal. The one-bit delay and subtracter blocks act as a differentiator. The output of the DSP demodulator and discriminator is then:

$$\Delta\varphi = \frac{d\varphi}{dt} = f \tag{2.2}$$

where f is the frequency which contains the information of the signal. Thus, the demodulation for the BFSK signal is accomplished.

2.4 Specification for the sample-and-hold circuit

Two critical components of the receiver are the sample-and-hold circuit and the limiting amplifier. This thesis concentrates on the design and implementation of the sample-and-hold circuit. In the following sections, the specification for the sample-and-hold circuit is presented.

The sample-and-hold circuit takes its input from the output of the anti-aliasing bandpass filter. The signal is centered at a frequency of 150.048 MHz, with a bandwidth of 100 kHz. This signal should be under-sampled with the sampling frequency of 1.152 MHz. At the output, the third harmonic is taken and fed to the analog-to-digital converter before passing to the DSP part of the receiver. From the previous discussion, we know that the output of the sample-and-hold circuit has a bandwidth of 100 kHz and a center frequency of 288 kHz.

The specifications of interest for the sample-and-hold circuit are dynamic range, aperture jitter, noise figure and power consumption. The sample-and-hold circuit must have a low aperture jitter in order not to introduce phase noise into the signal. The r.m.s. jitter should be less than 5 degrees of an IF cycle, in order to keep the phase noise under -30 dBc of the signal. Overall, the noise figure of the sample-and-hold circuit should add no more than 1 to 2 dB to the system noise figure. To satisfy the low-jitter requirement and to ensure that the circuit has a fast settling time during the sample-mode, the sampling rate of the sample-and-hold circuit is set to be 50 MHz for the design. The analog-to-digital converter following the sample-and-hold circuit should have an accuracy of 5-bits if the signal is limited. However, if the limiting amplifier does not saturate over

the whole dynamic range of the input signal, then the analog-to-digital converter must have more bits to compensate. As a result, the desired accuracy of the sample-and-hold circuit is set to be 8-bits. For the circuit to work in the receiver of a wireless communication system, power consumption is a concern. In base station applications, the sample-and-hold circuit should not consume more than about 25 mW at a supply voltage of 3 to 5V. In portable handset applications, the requirement is that the power consumption be no more than 10 mW for the sample-and-hold circuit at a supply voltage of 2.8 to 3V.

The specification for the sample-and-hold circuit is summarized in Table 2.1.

Table 2.1 Specifications for sample-and-hold circuit

Input signal frequency	150.048 MHz (Bandwidth = 100 kHz)
Sampling frequency	50 MHz
Accuracy	8 bits
RMS jitter	< 5 degrees of an IF cycle
Noise figure	2 dB
Power supply	3.3 V
Power consumption	< 10 mW

2.5 Summary

In this chapter, the application of the sample-and-hold circuit designed was introduced. The description of the CT2Plus personal communication radio was given, and requirements for the sample-and-hold circuit specified. In the next chapter, the background information for the sample-and-hold circuit is given. Based on that and information in this chapter, the design of a sample-and-hold decimator is presented in Chapter 4.

CHAPTER 3 Background

The sample-and-hold circuit is one of the key components in many data conversion systems, and has a significant impact on the overall performance of the system. As the speed and accuracy required by data conversion systems increase, a high-speed and high-accuracy sample-and-hold circuit is strongly desired.

Because of the need for portability, and concern about the cost of power supplies, reductions in supply voltage and power consumption are needed. Meanwhile, the speed and dynamic range of the circuit should not be sacrificed. As a result, current-mode circuits have increasingly gained interest due to their compatibility with low voltage operation and low power consumption.

In this chapter, various architectures of voltage-mode and current-mode sample-and-hold circuits are presented. Several perspectives, including speed, accuracy, and distortion are examined. Some approaches to reduce the errors are given, and practical limitations of each architecture are discussed. A comparison of the current-mode design with its voltage-mode counterpart is then provided. Two types of sampling switches, the bipolar-diode-bridge and the MOS-pass-transistor, are studied. They are then compared, and a preference is made.

3.1 Architecture

The basic function of a sample-and-hold system is to transform a continuous-time signal to a discrete-time signal. It is usually based on a voltage-memory device, often a capacitor, wherein a signal is sampled and stored periodically. During sample-mode (also called track-mode), the output signal tracks the input signal; during hold-mode, the signal value at the end of the sampling phase is held accurately.

3.1.1 Terminology

To avoid ambiguity, the terminologies commonly used to characterize the sample-and-hold system are first introduced below:

1. *Small-Signal Bandwidth* is the frequency at which the small-signal gain in the sample-mode falls 3 dB below its low-frequency value.

2. *Large-Signal Bandwidth* is the frequency at which the signal gain in the sample-mode falls 3 dB below its low frequency value, under an input condition of a full-scale sine wave.

3. *Acquisition-Time* is the time required for the voltage, held by the hold capacitor, to settle within a specified range of the input signal following a full-scale transition after the sampling command. Note that this is not necessarily the same as the output settling time. The maximum clock rate is only limited by the acquisition time, because it is only necessary that the hold-capacitor voltage should settle before transition to the hold-mode; the output can settle even after the operation is in the hold-mode.

4. *Aperture-Delay-Time* is the time between the hold command and the opening of the switch.

5. *Effective-Aperture-Delay-Time (EADT)* is the point in time, relative to the hold command, that the input signal is still being sampled. The aperture-delay-time is difficult to measure so EADT is usually measured instead.

6. *Aperture-Uncertainty-Time (Jitter)* is the variation in aperture-delay-time for successive

samples. Noise in the digital clock-drive circuit, switch noise, and the finite rise time of the clock signal contribute to this parameter.

7. *Pedestal Error* is the ratio of the induced voltage error, resulting from the transition from sample-mode to hold-mode, to the full-scale input voltage. For some architectures, this parameter might be a function of input signal. This error results from the sampling-switch injecting charge onto the hold capacitor when the hold command is asserted.

8. *Hold-Mode Settling Time* is the time between the assertion of a hold command and the time that the output voltage settles within a specified range of accuracy of its final value.

9. *Droop Rate* is the discharge rate of the holding capacitor during the hold mode.

3.1.2 Voltage-Mode Sample-and-Hold Circuit

There are two types of architectures for voltage-mode sample-and-hold systems: the open-loop architecture, and the closed-loop architecture. For each of them, there are several different configurations that provide different trade-offs between speed and accuracy.

The simplest open-loop sample-and-hold circuit is shown in Fig. 3.1. It consists of a sampling switch and a hold capacitor. When *clk* is high, the circuit operates in sample-mode; when *clk* is low, it operates in hold-mode. The output buffer separates the hold capacitor from the output load so as to provide the necessary output driving capability for the overall system. The switch is shown to be implemented with an MOS transistor.

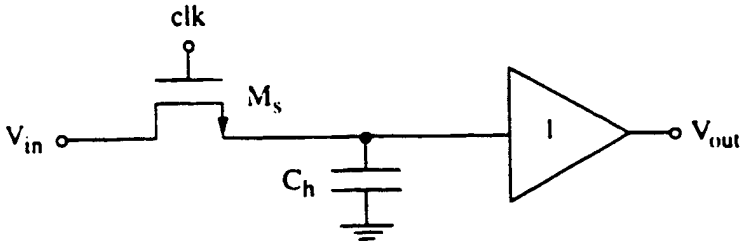


Figure 3.1 Open-loop sample-and-hold

This circuit can achieve very high speed because there is no feedback loop around it [7]. In

fact, the speed of the circuit is limited only by the bandwidth of the sampling switch and the bandwidth of the output buffer. However, the accuracy of this circuit is limited by two factors: a clock-feedthrough error introduced by the sampling switch at the high-to-low transition of the clock signal; and the fact that the offset, gain error, and nonlinearity of the unity-gain buffer and the sampling switch are not attenuated when referred back to the input. Notice also that both sides of the switch are at the signal level, thus the clock- feedthrough error is signal dependant. For the same reason, the switch opening time is influenced by the input signal, and results in a signal-dependent sampling jitter. This can cause severe distortion for large-amplitude input signals [8]. The clock-feedthrough error can be calculated according to Eq. (3.1).

$$\Delta V_{out} = -\frac{C_{ox}WL}{2C_h}(V_{DD} - V_{Tn} - V_{in}) - \frac{C_{ox}WL_{ov}}{C_h}(V_{DD} - V_{SS}) \qquad (3.1)$$

Here C_{ox} is the gate oxide capacitance per unit area of the MOS transistor M_s, W and L are the channel width and length of M_s correspondingly. V_{Tn} is the threshold voltage of M_s, L_{ov} represents the lateral diffusion of the drain and source junctions under the gate of M_s, and V_{DD} and V_{SS} are the two power rails for the clock signal.

A dummy switch can be added to the previous circuit to reduce the clock-feedthrough error as shown in Fig 3.2 [9]. Transistor M_1 has twice the width of M_2, and the gates of these

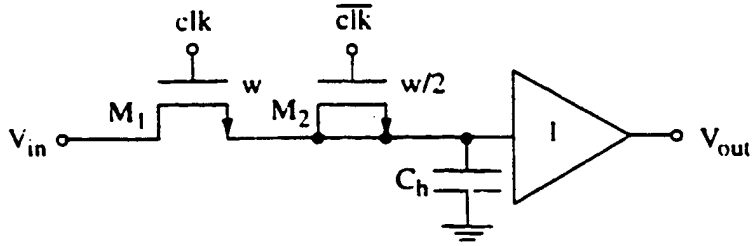


Figure 3.2 Using a dummy switch to cancel clock feedthrough

transistors are driven by non-overlapping complementary clock signals. Ideally, the clock-feedthrough error of the two transistors will be equal in magnitude, but opposite in sign, thus cancelling each other. However, the cancellation is never perfect due to the finite slope of the

clock signal and the mismatch between the two transistors. In fact, for ideal charge cancellation, the $\frac{W}{L}$ ratio of M_1 to M_2 should not be exactly 2:1. The required ratio is dependent on the rise and fall times of the clock signals and the threshold voltage of the transistors, and therefore is difficult to find. Nevertheless, if the clock signals are very fast, and $\overline{clk}$ goes high at the same time or slightly after clk goes low, the clock-feedthrough error will be partially cancelled.

Although the open-loop sample-and-hold system has the potential for high speed, its accuracy is limited. For higher accuracy, the closed-loop architecture can be used. Closed-loop sample-and-hold circuits utilize a feedback loop to achieve higher accuracy. One such configuration is shown in Fig 3.3 [11]. The two amplifiers provide a large loop-gain to reduce the closed-loop gain error and nonlinearity. The hold capacitor is now placed in the feedback path so that it is charged up through a relatively low-impedance virtual ground. The clock-feedthrough from the turn-off of the switch M_1 is now:

$$\Delta V_s = -\frac{C_{ox}WL}{2C_h}\left(V_{DD} - V_{Tn} - \frac{V_{in}}{A_2}\right) - \frac{C_{ox}WL_{ov}}{C_h}(V_{DD} - V_{SS}) \tag{3.2}$$

where A_2 is the open-loop gain of the second amplifier. For large A_2, the term $\frac{V_{in}}{A_2}$ can be ignored. The charge-injection error is now signal independent, and therefore is much more easily compensated with additional techniques.

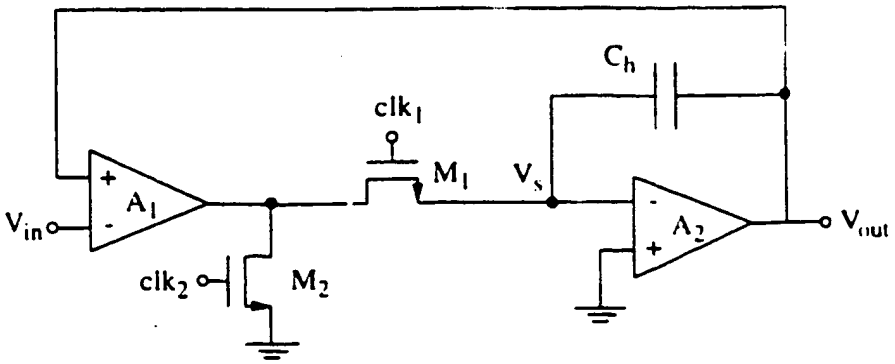


Figure 3.3 Closed-loop sample-and-hold circuit

An additional switch, M_2, placed to the left of the sampling switch, M_1, helps to improve feedthrough isolation [11]. Two complementary non-overlapping clocks ensure that M_1 and M_2

are never on at the same time. During hold mode M_2 clamps the output of the first amplifier to ground. With the proper switching sequence this circuit becomes parasitic insensitive [12][13].

Fig. 3.4 and 3.5 show two alternative configurations for closed-loop sample-and-hold circuits. The one in Fig. 3.4 reduces the clock-feedthrough error by employing a cancellation network at the positive input of the op-amp A_2 [14]. Ideally, the cancellation network generates a clock-feedthrough error which is the same as that at the negative terminal. If A_2 has good common-mode rejection, the error can be largely eliminated. However, due to the mismatch of the impedance levels at the left of switch M_1, and at the bottom of the switch M_2, the two feedthroughs are not exactly the same, so the cancellation is not perfect even with a *CMRR* of infinity.

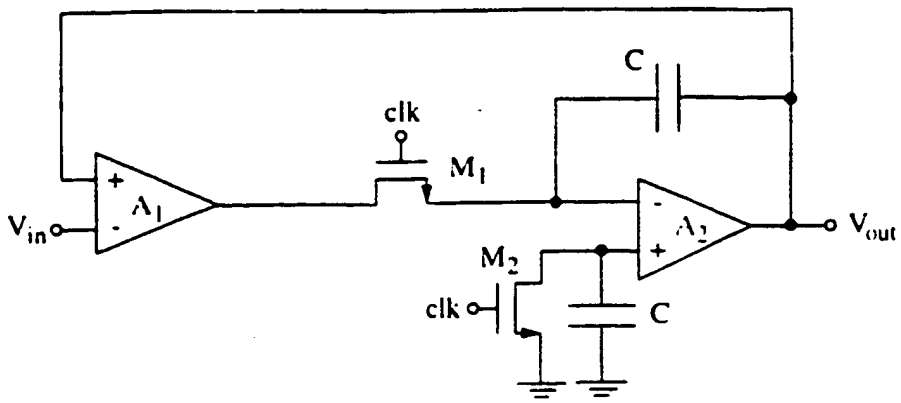


Figure 3.4 Closed-loop sample-and-hold circuit with feedthrough cancellation

The circuit in Fig. 3.5 reduces the clock-feedthrough error by using the fully differential structure [10][15]. Since the clock-feedthrough of each side is signal-independent, the feedthrough from the positive path should be the same as that from the negative path. Therefore, the differential output will be free of clock-feedthrough error. The cancellation is only affected by the matching of the components. One drawback of this approach is the increased circuit complexity, needing twice as many components as the single-ended version.

In the above discussion, it is shown that the open-loop configuration exhibits high speed while the accuracy is limited. On the other hand, the closed-loop configuration can achieve higher

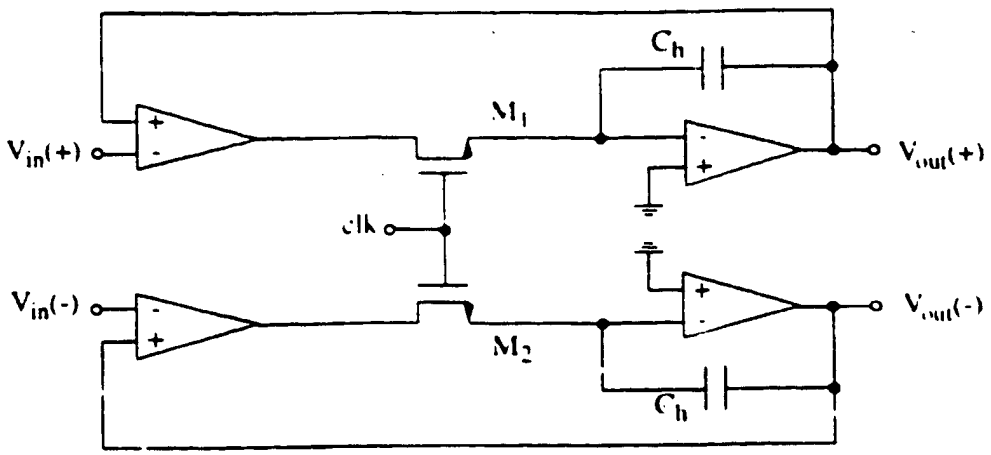


Figure 3.5 Closed-loop fully-differential sample-and-hold circuit

accuracy by the use of a feedback loop at the expense of reduced speed. Furthermore, due to the need for an adequate phase margin for good settling behavior in the closed-loop configurations, a low operating bandwidth results. This results in a long acquisition time and a limited input bandwidth. The use of more than two op-amps also increases the design complexity.

There are several other sample-and-hold circuits which improve the speed and accuracy of the circuit by taking advantage of the speed of the open-loop topology and the accuracy of the closed-loop topology [16]. In these topologies, the circuit operates as an open-loop structure in the sample-mode, and as a closed-loop structure in the hold-mode. However, these circuits use high supply voltage, consume more power, and are more complicated thus occupying a large chip area, therefore, they are not suitable for the design in this thesis.

3.1.3 Current Mode Sample-and-Hold Circuit

Since their first appearances [17][18][19][20][21], switched-current circuits have gained considerable interest for analog sampled-data signal processing, especially for high-speed, moderate-accuracy, and low-power applications. Compared to their voltage-mode counterparts, current-mode circuits have the advantages of being capable of operating at low supply voltages, consuming less power, having the potential of high speed, and occupying a smaller area. These

merits make them attractive candidates for portable applications. Several topologies for current-mode sample-and-hold circuits are presented below.

The simplest current-mode sample-and-hold circuit is shown in Fig. 3.6 [18]. It consists of

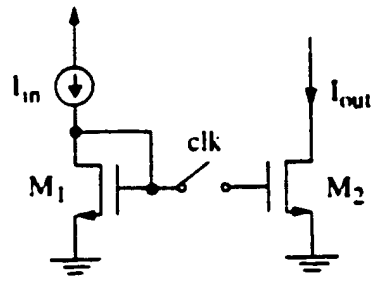


Figure 3.6 Current-Mode Sample-and-Hold

two MOS transistors and a sampling switch. In sample-mode, the switch is closed and the circuit acts as an MOS current mirror in which output current follows the input current. In hold-mode, the switch is open and the output current is held due to the charge trapped on the gate capacitor of M_2. One problem with this topology is that a mismatch between the two transistors results in an error in the output current. Two factors causing transistor mismatch are threshold voltage (V_T) mismatch and conductance-constant ($K = \mu CW/L$) mismatch [25]. They are both inversely proportional to the size of the transistor. In order to obtain a better matching, the W and L of the transistors should be large. However, from the small signal analysis, it is found that for a larger small-signal bandwidth, the transconductance g_m of the transistors should be as large as possible, and the gate capacitor should be as small as possible. Large g_m means that the $\frac{W}{L}$ ratio of the transistors should be large; and small gate capacitance means both W and L should be small. As a result, this trade-off between accuracy and bandwidth makes this topology inadequate for most applications. Another source of inaccuracy is the clock-feedthrough error introduced by the turn-off of the switch. With a MOSFET switch driven by a clock signal, this error can be expressed in Eq. (3.3). Here, ΔV_G is the clock-feedthrough caused by the turn-off of the switch to the gate of transistor M_2. Note that ΔV_G is signal dependent, therefore the feedthrough error at the output is

also signal dependent.

$$\Delta I_{out} = g_m \Delta V_G \tag{3.3}$$

To eliminate the matching problem, the circuit in Fig. 3.7 can be used [17][18][20][22].

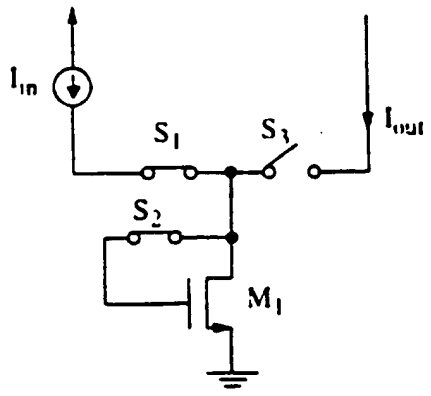


Figure 3.7 Dynamic current mirror as a sample-and-hold circuit

Transistor matching is no longer a problem since now only one transistor is used. During sample-mode, switches S_1 and S_2 are closed, and switch S_3 is open. Input current flows into transistor M_1. During hold mode, S_1 and S_2 are open while S_3 is closed. The value I_{out} is equal to the value of I_{in} at the end of the sampling interval due to the charge trapped on the gate capacitor of M_1. Although the accuracy of this design is not affected by component-matching as in the previous case, it is still affected by two factors: the signal dependent clock-feedthrough, and the finite output resistance of the MOS transistor. This finite output resistance introduces an error in the output current whenever there is a voltage difference between the input and output nodes. From a small-signal analysis, the input-output relation can be expressed as:

$$\frac{i_{in}}{i_{out}} = \frac{r_o}{r_o + 1/g_m} \tag{3.4}$$

There are two traditional approaches used to increase the output resistance of the transistor. One is to use long channel devices, the other is to use a cascode configuration. Neither of these is suitable for high-speed and high-accuracy operation when using small power-supply voltages. The use of long channel devices reduces the speed of the circuit greatly, while the use of

a cascode configuration reduces the allowable voltage swings, which in turn leads to a reduced current dynamic range.

To eliminate the error in the output current caused by the finite output resistance, active negative feedback can be used (Fig. 3.8) [21]. From small signal analysis, it can be shown that:

$$\frac{i_{in}}{i_{out}} = \frac{r_o}{r_o + 1/(Ag_m)} \tag{3.5}$$

Active-negative feedback reduces the current mismatch caused by the transistor's finite output impedance by a factor of $\frac{1}{A}$.

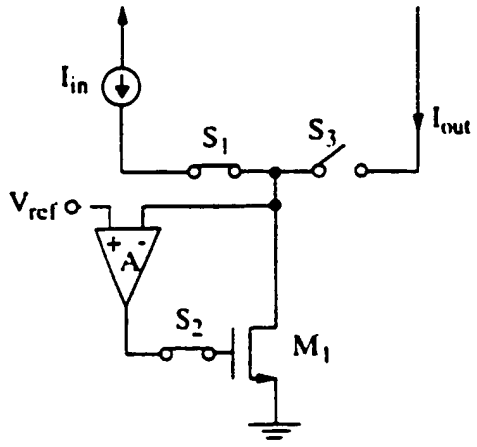


Figure 3.8 Switched-current sample-and-hold with active-negative feedback

The amplifier in the above circuit can be implemented using either a common-source amplifier or a common-gate amplifier. It was shown in [23] that with a similar bias condition and under the same stability criterion (i.e. identical Q factors), the common-gate amplifier based circuit provides a higher bandwidth, and therefore is more suitable for high speed operation.

This design still has the charge-injection error. A fully-differential structure can be used to reduce the signal-independent part of the charge-injection error and any offset current [24].

3.2 Comparison of Voltage-Mode and Current-Mode Circuits

Traditionally, electronic signals are processed in voltage-mode. However, as the demand for low supply voltage, high speed, and low power consumption increases, current-mode design is starting to gain more popularity.

For voltage-mode circuits, the dynamic range of the circuit is greatly reduced as the power-supply-voltage is lowered. In current-mode design, however, the dynamic range of the circuit is not significantly affected by a reduction in supply voltage because the signal is now represented by current instead of by voltage.

In current-mode design, voltages do not have to change much. Consequently, the parasitic capacitances which limit the speed of the voltage-mode design do not need to be charged up or discharged constantly. Therefore, the speed of a current-mode circuit can be much higher than that of a voltage-mode circuit.

To perform a certain function in current-mode may be simpler than that in voltage-mode. High-gain amplifiers are usually not needed, current addition and subtraction can be performed easily, and ratioed current-mirrors can be used to provide scaled current. One drawback of the current-mode circuit, however, is that to provide a current signal to more than one node, additional parts (e.g. current mirrors) are needed; in a voltage-mode circuit, this can be easily done by connecting the voltage signal directly to all the nodes that require the signal.

3.3 Switches

In an analog sampling system, the sampling switch plays an important role in determining the overall performance of the system. There are many types of analog switches over a wide variety of device and circuit configurations. Differential pairs, either Bipolar or MOS, can be used as current switches; diode-bridge configurations can act as switches; unipolar devices, including MESFET, JFET, and MOS pass transistors can also be operated as analog switches. Among them, MOS switches and bipolar diode-bridge switches are the most attractive when BiCMOS

technology is used. Until now, the use of MOS switches was assumed. In the following sections, both the MOS and diode bridge switches will be examined in more detail, and a comparison of their performances will be made.

3.3.1 Diode-Bridge Switch

Fig. 3.9 shows a simplified schematic of one type of diode bridge. During sample-mode, matched current sources I_1 and I_2 are turned on so as to turn the diodes on and generate a low impedance path between the input and output nodes. The hold capacitor is charged up until the currents in the two output diodes are the same. In the ideal case, the output voltage and the input voltage are the same at this point. However, there are several sources of errors. The mismatch among diodes in the bridge causes offset errors. The mismatch between current sources I_1 and I_2 introduces another source of error. In addition, switching-time mismatch between I_1 and I_2 causes charge injection onto the holding capacitor.

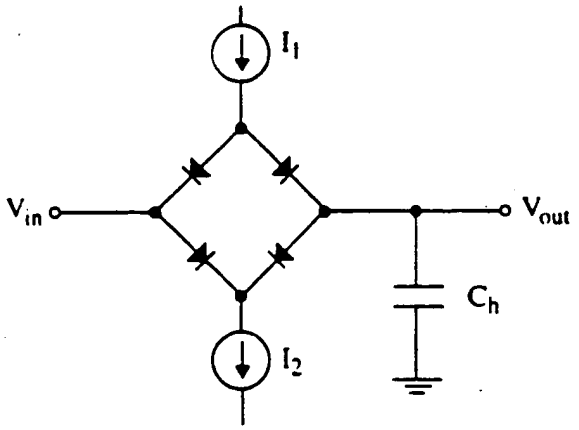


Figure 3.9 Diode-Bridge as a Switch

When the diode bridge is fabricated within a monolithic integrated circuit, the parasitic capacitances associated with the diodes degrade the switching speed and increase pedestal error as well [26].

3.3.2 MOS Switch

For the MOS switches, there are two principal sources of errors: one is gate overlap

capacitance, and the other is trapped channel charges during fast turn-off [27]. This charge injection phenomenon of the MOS transistor can be described qualitatively as follows. A finite quantity of mobile carriers exist in the channel when an MOS transistor conducts. When the transistor is turned off, the rapid variation of the gate voltage causes a variation of the surface potential as the quantity of mobile charges cannot change instantaneously [28]. An equilibrium corresponding to the new gate voltage is reached by the charge flowing to the source, the drain, and the substrate electrodes. The charge transferred to the output node during the switch turn-off period adds an error component to the sampled voltage. In addition, the charge associated with the feedthrough effect of the gate-to-diffusion overlap capacitance enlarges the error voltage even after the switch is turned off.

Fig. 3.10 illustrates an NMOS switch turning off by a clock signal falling from V_H to V_L.

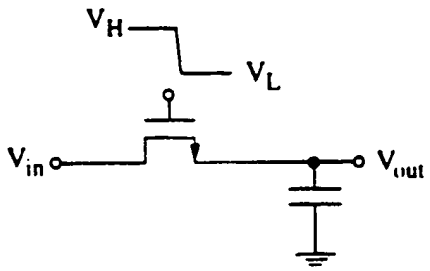


Figure 3.10 NMOS Switch

For very fast clock waveforms, the total error caused by trapped channel charge is approximately given by:

$$\Delta V_{o1} = -\frac{C_{ox}WL}{2C_h}(V_H - V_T - V_{in}) \tag{3.6}$$

The error voltage caused by the overlap capacitance is:

$$\Delta V_{o2} = -\frac{C_{ox}WL_{ov}}{C_h}(V_H - V_L) \tag{3.7}$$

Therefore, the total clock-feedthrough error onto the hold capacitor is:

$$\Delta V_o = (\Delta V_{o1} + \Delta V_{o2}) \tag{3.8}$$

With a CMOS switch driven by complementary clock signals (Fig. 3.11), the clock feedthrough error can in theory be cancelled completely if both PMOS and NMOS transistor have

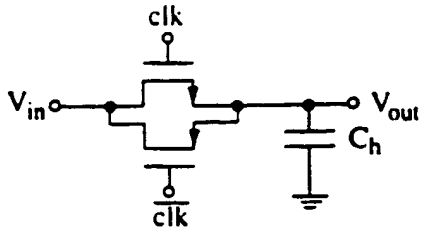


Figure 3.11 CMOS Switch

the same size and same threshold voltage. However, this is true only when the input signal is half way between the positive and negative rail of the clock signal. In addition, two major problems exist: the mismatch of the threshold voltage and size of the transistors, and the fact that it is not possible to make exactly symmetric complementary clock signals.

3.3.3 MOS Switch vs. Diode Bridge Switch

The performance of a sampling switch can be represented by its sampling bandwidth, its pedestal error, and its distortion. The above two basic sampling switch topologies, a MOSFET implementation and a bipolar implementation, are evaluated and compared in the following section.

For an open-loop system, the sampling-switch bandwidth has a direct impact on the speed of the overall system. The sampling-switch bandwidth for an MOS transistor is determined by its on resistance and the hold capacitor according to Eq. (3.9). For the diode-bridge switch, the bandwidth is limited by the drive current I_1 and I_2 for charging and discharging the hold capacitor.

$$B = \frac{1}{2\pi R_{on} C_h} \tag{3.9}$$

From the discussions in the previous sections, it is found that for the MOS switch, the

sampled pedestal is dominated by the charge-injection phenomenon. The sampled pedestal of the diode bridge is mainly determined by the diode mismatches. It can be reduced by minimizing the bias current. Therefore, for the diode bridge, there is a trade-off between sampling switch bandwidth and pedestal error.

Compared to the MOS switch, the diode bridge operates on lower-level clocks [29]. Therefore, the diode bridge potentially offers better sampled pedestal and aperture jitter performance than the MOS switch.

For MOS switches, the interference between control (clk) and the signal is only significant at the high-to-low transition of the clock signal. For diode-bridge switches, control and signal are "DC-coupled"; that is, any low frequency noise and drift of the control signal will be imposed on the signal.

The diode bridge switch has more sources of error compared to the MOS switch. ·rnore, its performance is dependent on the element matching while in case of an MOS mismatch-dependent performance does not exist. In addition, there are many existing .. ues to reduce the charge injection problem of the MOS switch including the use of dummy switches, compensation networks, and fully differential structures.

3.4 Summary

For the reasons given in this chapter, a current-mode sample-and-hold circuit with active-negative feedback was chosen to realize the sample-and-hold circuit. Single NMOS or PMOS transistors are used to implement the switches for the reason of simplicity. Dummy switches and a fully-differential structure are used to reduce the charge-injection error and other nonlinearities.

CHAPTER 4 Circuits

In this chapter, the design of the sample-and-hold circuit is described. First, the requirements for the behavior of the sample-and-hold circuit are given, then an appropriate architecture is selected. Various design considerations are examined, and simulation results are given.

4.1 Requirements

In Chapter 2, a detailed description of the application and specifications for the sample-and-hold circuit was given. A summary of the requirements for the sample-and-hold circuit can be found in Table 2.1.

The major design specification for the sample-and-hold circuit requires that the circuit operates with a 3.3V power supply, has a sampling frequency of 50 MHz, has an accuracy of more than 8 bits, and consumes less than 10 mW power.

4.2 Architecture

Chapter 3 contains the background information of various architectures for sample-and-

hold circuits. Consider the specification for the sample-and-hold circuit, the current-mode architecture with active-negative feedback is chosen for the design. With BiCMOS technology, the speed of bipolar devices can be combined with the excellent hold capability of MOS devices to achieve the best performance. A fully differential structure is used to reduce clock-feedthrough error and total harmonic distortion.

4.3 Circuit

In Chapter 3, Fig. 3.8, a functional block diagram of the sample-and-hold circuit was presented. In the following sections, several issues, including implementation of the active-negative feedback amplifier, realization of the switches, use of a fully differential structure, generation of the clock signals, and the dynamic range of the circuit, are discussed in more detail.

4.3.1 Active-Negative Feedback

In this design, the common-gate topology is adopted to implement the active-negative feedback. With the BiCMOS process, modifications are made such that the amplifier is implemented with a single bipolar transistor in a common-base configuration. The sample-and-hold circuit with the amplifier is shown in Fig. 4.1. Compared with an MOS implementation, the use of a bipolar transistor results in improved speed and frequency response of the circuit since bipolar transistors have a higher transconductance, g_m, than MOS transistors.

The operation of the circuit is as follows. On clock phase ϕ_1, switches S_1 and S_2 are closed, while S_3 is open; a current signal i flows from the emitter of the common-base transistor Q_1 and charges up the hold capacitor C_h. As the voltage on C_h changes, the current in transistor M_2 changes correspondingly until it reaches the value $I + i$. At this time, the current in Q_1 returns to the bias current I. Note that the voltage at the input node is close to a constant value $V_{in} = V_{ref} - V_{be}$ where V_{be} is the base-emitter voltage of Q_1 when I_c of Q_1 is I. Thus, a virtual ground is created at the input node, which means a low effective input-impedance, therefore a high current transfer ratio for a current-mode circuit. On clock phase ϕ_2, switches S_1 and S_2 are

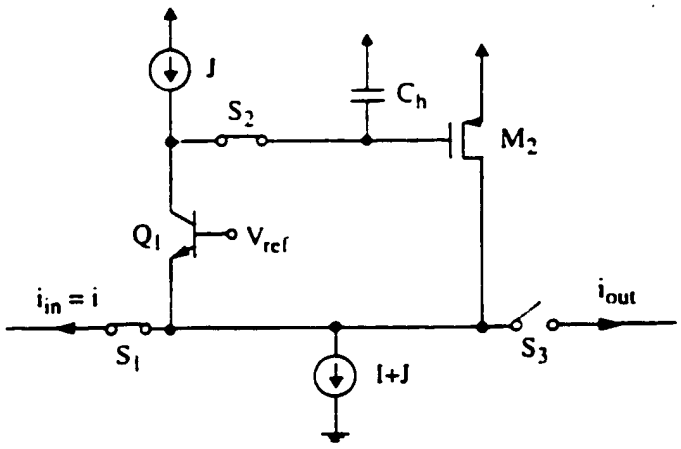


Figure 4.1 Current-mode BiCMOS sample-and-hold circuit

open while S_3 is closed. The feedback loop is broken, and the current in transistor M_2 sustains the value $I + i$ due to the charge trapped on the h old capacitor (assuming leakage current can be ignored); the output current will then have the value i.

Small-signal analysis is performed to examine the frequency response of the circuit in sample-mode. The small-signal equivalent circuit of the sample-and-hold circuit in sample-mode is shown in Fig. 4.2.

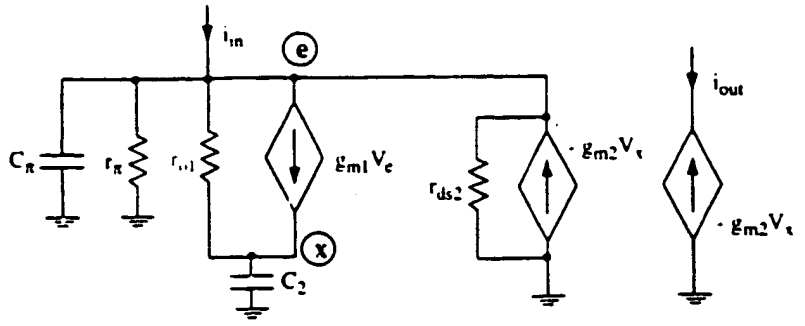


Figure 4.2 Small signal model for the current-mode sample-and-hold circuit

From the diagram, the transfer function is found to be:

$$\frac{i_{out}}{i_{in}}(s) = \frac{N(s)}{D(s)} \tag{4.1}$$

where

$$N(s) = (g_{m1}g_{m2}) / (r_{o1}r_{o2})$$

and

$$D(s) = s^2 + \left(\frac{r_{o1}r_{ds2}C_2\left(g_{m1} + \frac{1}{r_\pi}\right) + C_2 r_{o1} + C_1 r_{ds2} + C_2 r_{ds2}}{C_1 C_2 r_{o1} r_{ds2}} \right) s + \frac{1 + \left(g_{m2} + \frac{1}{r_\pi}\right) r_{ds2} + g_{m1} g_{m2} r_{o1} r_{ds2}}{C_1 C_2 r_{o1} r_{ds2}}$$

Here, $C_1 = C_\pi$, $C_2 = C_{gs2} + C_h$, g_{m1} and r_{o1} are the transconductance and output resistance of transistor Q_1, while g_{m2} and r_{ds2} are the transconductance and drain-to-source resistance of transistor M_2.

Recall that the denominator of a second order system can be expressed in the form:

$$D(s) = s^2 + \frac{\omega_o}{Q} s + \omega_o^2 \tag{4.2}$$

where ω_o is the pole frequency, and Q is the pole Q factor. From these two parameters, the frequency response of a system can be observed.

Comparing Eq. (4.2) with Eq. (4.1), and assuming $g_{m1}r_{o1} \gg 1$ and $g_{m2}r_{ds2} \gg 1$, it can be concluded that, for the sample-and-hold circuit operating in sample-mode,

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}} \tag{4.3}$$

$$Q = \sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}} \tag{4.4}$$

The pole frequency ω_o is the radial distance of the poles on a complex plane; for the $-3dB$-bandwidth to be large, ω_o should be as large as possible. The pole Q-factor indicates the distance of the poles from the $j\omega$-axis, and therefore it determines the stability and settling behavior of the system. The desirable frequency response of the sample-and-hold system should have no peaking so as to result in a faster settling. In order to satisfy this requirement, the Q factor should not be more than $\frac{\sqrt{2}}{2}$.

The frequency response of the two-pole system can also be examined by finding the two poles of the system. Note that when the poles are real and widely spread, the denominator of the

transfer function can be written as:

$$D(s) = 1 + \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{4.5}$$

where p_1 and p_2 are the two dominant poles of the system. In order for the poles to be real, the value for Q should not exceed $\frac{1}{2}$. According to Eq. (4.4), this means that $\sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}}$ should not exceed $\frac{1}{2}$.

Comparing Eq. (4.5) to Eq.(4.2), the two dominant poles for this circuit can be expressed as:

$$p_1 = \omega_u Q = \frac{g_{m2}}{C_2} \tag{4.6}$$

and

$$p_2 = \frac{\omega_u}{Q} = \frac{g_{m1}}{C_1} \tag{4.7}$$

The first pole determines the small-signal bandwidth of the circuit; therefore, for a large $3dB$ bandwidth, p_1 should be large. For the system to have good stability, the second pole has to be large.

From Eq. (4.3), (4.4), (4.6), and (4.7), it can be concluded that proper selection of sizes for transistors and capacitors is actually a trade-off between settling behavior and signal bandwidth. All these factors should be taken into account when proper sizes for transistors Q_1, M_2, and capacitor C_h are chosen. HSPICE simulation can be used to assist in choosing the component sizes. This will be discussed in more details in section 4.4.1.

4.3.2 Switches

There are three switches in this circuit: the sampling switch, the input switch, and the output switch.

The sampling switch has a strong impact on the maximum achievable clock frequency and the charge-injection error. In this design, for reasons of simplicity, an NMOS transistor is used to

realize this switch.

For MOS switches, trade-off occurs between achievable maximum clock frequency and charge-injection error when sizes of the switches are varied.

The acquisition time of the sampling system consists of two parts: the switch turn-on time, which is determined by the internal propagation delay of the switch; and the time to charge up the capacitor to the desired value [30]. For small hold capacitors, the sampling switch can be modelled as a pure resistor for the purpose of estimating the charge-up time of the capacitor. The value of the resistor is equal to the maximum on-resistance of the switch. This simple system has an exponential step response; therefore, the time for the output to settle to a value near the input signal also depends on the desired accuracy of the system. For example, if 12-bit accuracy is required, the time required for the output value to sett[le] ...al to nine time constants, $9 \times RC$, where R is the on-resistance of the switch, and C is t[he] ... capacitor. As a result, a small time constant, RC, is required to ensure that the switch settlin[g] ... will not impose a limitation on the acquisition time of the sampling system, and hence will no[t] ...ffect the maximum clock frequency.

From the previous discussion, it is evident that for a high clock frequency, the on-resistance of the transistor must be small; therefore the switch transistor's $\frac{W}{L}$ ratio must be large. However, when the clock-feedthrough error is considered, the size of the switch is required to be small. In addition, a smaller on-resistance (larger transistor) results in a higher droop rate due to larger leakage current at the switch's source and drain. This kind of trade-off between speed and accuracy is not uncommon. Appropriate values for the switch sizes must be chosen to meet the system specifications. Hand calculation was first used to get an upper limit on the sampling switch size for a maximum clock frequency of 100 MHz (which ensures that the circuit functions properly when sampled at 50 MHz as required) and a lower limit on the switch size for an accuracy of 10 bits. HSPICE simulation was then performed to find suitable values for the sizes of the sampling switches.

Minimum length transistors were used to implement the sampling switches. The dummy-

switch approach was used to help reduce the charge-injection errors. The aim is to get an acquisition time of less than 10 ns, which corresponds to a maximum sampling rate of more than 50 MHz, and an accuracy of 10 bits.

Input and output switches are needed to deliver current signals. For this purpose, MOS differential pairs are used. When a relatively small-difference voltage is applied to the gates of an MOS differential pair, the source current will flow almost entirely in one of the two transistors. Therefore, differential pairs display excellent current-switching capability. The differential voltage applied to the gates of the differential pair can be relatively small so as not to introduce extra errors from charge-injection; in addition, this results in smaller voltage swings at the circuit's internal nodes which is important when the design is to be operated with low power supply voltage.

4.3.3 Fully-Differential Circuit

Fully-differential structure has a number of advantages over single-ended structure, and is relatively immune to noise, has smaller harmonic distortion (even order harmonics are cancelled at the output), rejects common-mode signals at the output, and for the switched-current circuit, it reduces clock feedthrough error. Another advantage of fully-differential circuits is that an inversion can be achieved by simply interchanging the two input lines.

In this design, the fully-differential structure is adopted. The circuit is shown in Fig. 4.3. It is derived directly from the single-ended version of the circuit.

The operation of the circuit can be explained as follows. Each of the half circuits operates in the same manner as that of the single-ended circuit. In the following discussion, a positive current signal is defined as a current which enters a node, while a negative current signal is a current which leaves a node. The positive branch takes the positive current signal i_{in+} as the input, and produces the positive output signal i_{out+} ; the negative branch takes the negative current signal i_{in-} as the input and produces the negative output signal i_{out-} . The differential

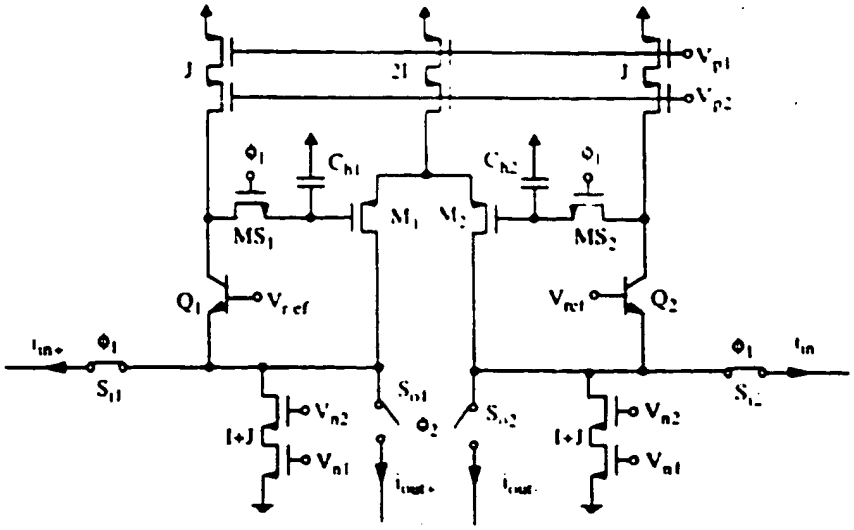


Figure 4.3 Current-mode fully-differential sample-and-hold circuit

input signal is then $i_{in+} - i_{in-}$, and the differential output signal is $i_{out+} - i_{out-}$. The maximum current achievable at the output depends on the current in the current sources. For the situation depicted in the diagram, where the current in the current source to the two hold transistors is $2I$, the maximum differential output signal cannot exceed $2I$.

When designing the circuit, in order to maintain the power dissipation in the fully-differential version the same as that in the single-ended version, the current level in each side of the circuit is halved compared to that in the single-ended circuit. However, the speed of the sampling operation is determined by the charging and discharging rates of the hold capacitors. Both the current level and the sizes of the hold capacitors affect this speed (Eq. (4.8)).

$$\frac{dV}{dt} = \frac{I}{C_h} \tag{4.8}$$

Therefore, for the fully-differential circuit, in order not to reduce the speed of operation, the sizes of the hold capacitors are half of that in the single-ended version.

High-swing current mirrors are used to implement the current sources in the circuit because they have both high output impedance and high output voltage swing. In addition, the bias circuit for the current sources consumes very little power and is suitable for low voltage and

low power consumption operation.

For a clock signal swing from V_{ss} to V_{dd}, ignoring the mismatches between the transistors M_1 and M_2, the clock-feedthrough error for the sample-and-hold circuit is:

$$\Delta I_{out} = K_m\left[-\frac{C_{ox}W_sL_s}{2C_h}\left(\sqrt{\frac{I+i_{in+}}{K/2}}-\sqrt{\frac{I+i_{in-}}{K/2}}\right)\right] \tag{4.9}$$

where W_s and L_s are the width and length of the switches MS_1 and MS_2, g_m is the small signal transconductance of the MOS hold transistors, K is the conductance constant of the hold transistors and has the value $(\mu_p C_{ox}\frac{W}{L})$, C_h is the capacitance of the hold capacitors, I is the bias current in transistors M_1 and M_2, and i_{in+} and i_{in-} are the positive and negative input current signals respectively.

In the previous chapter, it was shown that the clock-feedthrough error of the single-sided version of the switched-current sample-and-hold circuit is signal-dependent. Note that when the single-sided circuit has a signal-dependent clock feedthrough, only the signal-independent part of the clock-feedthrough is cancelled in its corresponding fully-differential circuit. Therefore, the signal dependent part of the clock-feedthrough error still exists in this fully-differential sample-and-hold circuit. In addition, mismatches between transistors M_1 and M_2 and between capacitors C_{h1} and C_{h2} cause the signal-independent part of the clock feedthrough error to be cancelled only partially. For this reason, dummy-switches are added to further reduce the clock-feedthrough error.

One problem with this fully-differential circuit is that a common-mode input signal tends to affect the operation of the circuit. It shifts the operating points of transistors and causes them to operate in undesired regions. This problem, and the method chosen to solve it, will be discussed in more detail in section 4.3.4.

Another potential problem with the fully-differential circuit is the error caused by component-mismatch. Due to process variations, mismatches exist between the supposedly identical capacitors C_{h1} and C_{h2}, hold transistors M_1 and M_2, and current sources.

In the context of the expression for clock feedthrough error (Eq. (4.9)), the capacitance-mismatch leads to an additional error in the output current (Eq. (4.10)). Layout techniques can be used to improve matching between the capacitors; the details can be found in chapter 5.

$$\Delta I_{out} = g_m \left(\frac{1}{C_{h1}} - \frac{1}{C_{h2}}\right)\left[-\frac{C_{ox}WL}{2}\left(\sqrt{\frac{I+I_{in}}{K/2}} - \sqrt{\frac{I+I_{in}}{K/2}}\right) - C_{ox}WL_{ov}(V_{dd} - V_{ss})\right] \qquad (4.10)$$

Two factors contribute to the drain current mismatch of MOS transistors: threshold voltage mismatch and conductance constant mismatch. The standard deviation of the threshold voltage mismatch is inversely proportional to the square root of the effective channel area. The mismatch in conductance constant due to edge variations is proportional to $\left(\frac{1}{L^2} + \frac{1}{W^2}\right)^{1/2}$; for N-channel devices, this is the dominant source of mismatch; P-channel devices have a larger mismatch in conductance constant, likely due to the poorer gate oxide capacitance matching compared to N-channel devices. Another reason could be that they have a larger mobility variation [31]. The study of these effects on the overall performance of the circuit is presented below.

From the above discussion, it is evident that both of the mismatches from threshold voltage mismatch and conductance constant mismatch are smaller when the effective width and length of the devices are larger. Therefore, for the mismatch between the two hold transistors to be small, the width and length of M_1 and M_2 must be large. However, for high-speed operation, the gate capacitances of both of the devices must be small, which in turn means small transistor widths and lengths; also, the transconductance, g_m, of the transistors must be large to achieve high-speed operation, which in turn requires a large transistor $\frac{W}{L}$ ratio. Therefore, the sizes of the transistors determine the trade-off between speed and accuracy.

High swing current mirrors are used as current sources in this design. Mismatches between the supposedly identical current sources result in an error in the output current. Fig. 4.4 contains a diagram of a high swing current mirror.

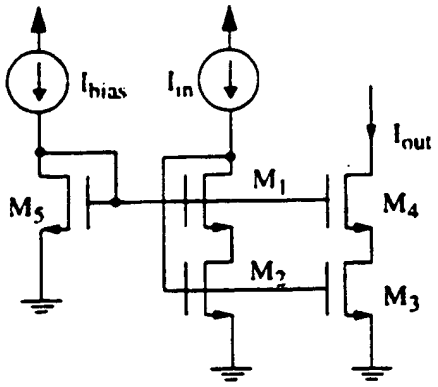


Figure 4.4 High swing current mirror

Analysis of the mismatch in the mirror leads to the following equation [32]:

$$\frac{\Delta I}{I_{in}} = \frac{I_{out} - I_{in}}{I_{in}} = \frac{\Delta K}{K_{21}} - 2\Delta V_T \left(\frac{K_{21}}{I_{in}}\right)^{\frac{1}{2}}$$

where

$$\Delta K = K_2 - K_1 \qquad (4.11)$$

$$\Delta V_T = V_{T2} - V_{T1}$$

$$K_{21} = \frac{K_2 + K_1}{2}$$

From the equation, it can be seen that both threshold mismatch and conductance constant mismatch contribute to the mismatch between input and output currents. It can also be seen that the two mirroring devices, M_2 and M_1, determine the mismatch. Therefore, they need to have large channel areas. When the finite output resistance, r_o, is considered, the mismatches in the upper two transistors M_1 and M_4 result in a difference in the drain-to-source voltage in the mirroring device, and therefore add an additional mismatch to the output current. However, it is insignificant compared to the error caused by the mismatch between the mirroring devices. From the equation, notice also that the input current level has an effect on the output current mismatch.

To minimize the problem of component mismatch while not degrading the performance of the system, component sizes must be chosen properly. HSPICE simulation is used to assist in

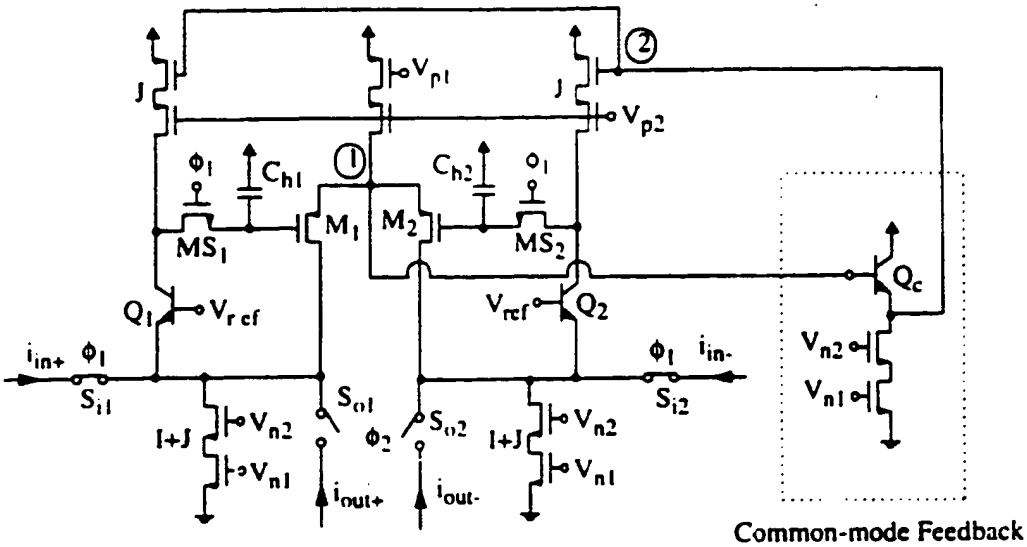
choosing the component sizes. Furthermore, layout techniques can be used to reduce the effects of mismatches as will be discussed in Chapter 5.

4.3.4 Common-mode Feedback Circuitry

It is found that the fully-differential circuit operating in sample-mode is sensitive to common-mode signals. When common-mode signals exist, the operating points of the transistors M_1, M_2, Q_1, and Q_2 are shifted; this leads to improper operation of the circuit. To clarify this, two extreme cases are presented as follows. First, consider the case where a DC common-mode current signal I_{cm} goes into the input nodes. The DC bias currents I_{sd1} and I_{sd2} in transistors M_1 and M_2 are reduced; and if $I_{cm} = I$ (where I is the bias current for transistors M_1 and M_2), both of these transistors are cut off. Next, consider the case where a DC common-mode signal I_{cm} goes out of the input nodes. I_{sd1} and I_{sd2} are increased, and this in turn pulls down the voltage at the sources of M_1 and M_2. When the voltage at the sources of M_1 and M_2 becomes lower than the reference voltage V_{ref} at the bases of the bipolar transistors Q_1 and Q_2, these two transistors saturate; as a result, the circuit cannot operate properly. Therefore, for the circuit to operate correctly, a common-mode feedback circuit is required to reject the common-mode signals.

In order not to increase the circuit complexity and power consumption, a simple configuration is utilized to reject the common-mode signals. The circuit including the common-mode feedback portion is shown in Fig. 4.5. The basic idea is to use the voltage at node 1 as a control signal, feed it back to node 2. The negative feedback around the loop ensures that currents from the two top current sources for the bipolar transistors settle to the proper values to compensate the common-mode input signals, and therefore maintain the current level in the hold transistors M_1 and M_2 at I.

Examining the sample-and-hold circuit, it is found that in normal operation, the voltage level at node 1 is higher than that at node 2. This can be explained by an analysis of the high-swing current-mirror [33]. One such mirror is shown in Fig. 4.4. For the mirror to operate



Device sizes & bias current values:

	M_1,M_2	MS_1,MS_2	C_{h1},C_{h2}	Q_1,Q_2,Q_c	I	J
W(μm)	40	16	0.65 pF	1x	0.55 mA	0.3 mA
L(μm)	1.2	0.8				

Figure 4.5 Fully differential sample-and-hold with common-mode feedback

properly, the following condition must be satisfied:

$$V_{out} > 2(V_{gs} - V_T) \tag{4.12}$$

where V_{gs} is the gate-to-source voltage of the mirroring device M_1. As a result, V_{out} can be lower than V_{gs}.

When PMOS transistors are used to construct the mirrors instead of NMOS transistors, a condition complementary to the one in Eq. (4.12) holds.

$$V_{dd} - V_{out} > 2(V_{sg} - |V_T|) \tag{4.13}$$

In this design, from the simulation, it is found that the voltage at node 1 is about 0.8V above the voltage at node 2. Therefore, for the common-mode feedback circuitry to operate correctly, some form of level shifting is required before feeding the voltage at node 1 to node 2. In this case, one diode voltage drop is required. Considering the required speed of the circuit, the base-emitter junction of a bipolar transistor Q_{cm} is used to achieve this. The transistor is configured as a source

follower. It has the advantages of preserving the speed of the circuit, consuming little power, and occupying a small area.

The operation of the common-mode feedback circuit is as follows. When the common-mode current signal flows into the input nodes, the voltage at node 1 goes up; this voltage is fed back to node 2 through a source-follower connected bipolar transistor, and as the voltage at node 2 goes up, the currents from the current sources decrease to compensate for the common-mode current signal, and consequently the currents in transistors M_1 and M_2 are preserved. On the other hand, when the common-mode current signal flows out of the input nodes, the voltage at node 1 is pulled down; when this voltage is fed back to node 2, currents from the current sources increase; as a result, currents in Q_1 and Q_2 go down, which in turn keeps the currents in hold transistors M_1 and M_2 constant. As a result, the common-mode signal is rejected.

The range of the common-mode signal is limited by the stability criterion as well as the value of the second pole of the circuit. According to Eq. (4.4) and Eq. (4.7), in order for Q to be less than $\frac{\sqrt{2}}{2}$ and for the second pole to be large enough, a lower limit on g_m of transistors Q_1 and Q_2 exists. Therefore, there is a lower limit on the bias current in Q_1 and Q_2.

4.3.5 Bias Circuit

The bias circuit in Fig.4.6 is used to bias the sample-and-hold circuit. This bias circuit combines the wide-swing cascode current mirrors with constant g_m bias circuit. By doing so, this circuit has the advantage of being capable of low power supply voltage operation; and, to a first order approximation, it eliminates errors due to the finite output impedance of transistors [33]. Another advantage of this bias circuit is that it has a low power consumption, since the bias current in each transistor can be as low as a few μA. An off chip resistor is used for R so that it can be trimmed to get the desired bias current levels during testing.

One thing to notice about this circuit is that it has two stable operating points, and one of them is the zero-state. Therefore, in order to get the circuit work, some start-up circuitry is

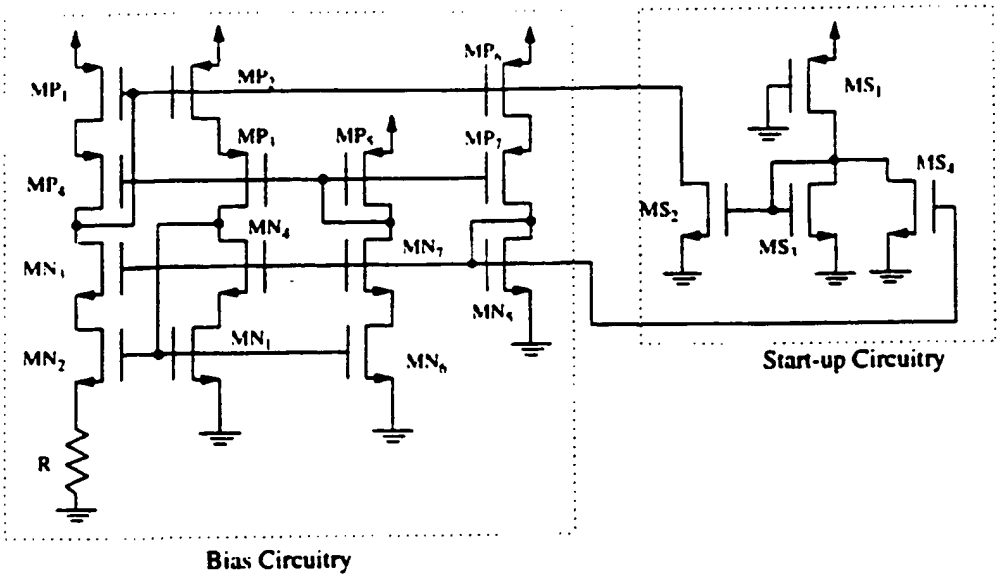


Figure 4.6 Bias circuit with start-up circuitry

required. The start-up circuit works in such a way that when the bias circuit is in zero-state, the start-up circuit is operating and supplying current to the bias circuit; however, once the bias circuit leaves the zero-state, the start-up circuit is disabled. As a result, the start-up circuit does not have any impact on the bias circuit during operation.

One type of start-up circuit is included in Fig. 4.6. The $\frac{W}{L}$ ratio of MS_4 is much larger than that of MS_3. The operation of the circuit can be explained as follows. When the bias circuit is in the zero-state there is no current in it, therefore the voltage at the gate of the transistor MP_1 is V_{dd}, and the voltage at the gate of MN_5 is zero. Transistor MS_2 turns on and transistor MS_4 remains off. The voltage at the gate of transistor MP_1 discharges through transistor MS_2, and when this voltage is low enough, transistor MP_1 turns on, and the bias circuit leaves the zero-state and starts to work. At this time, the voltage at the gate of MS_4 is equal to V_{gs} of transistor MN_5, therefore, MS_4 turns on. Since the $\frac{W}{L}$ ratio of MS_4 is much larger than that of MS_3, the current supplied by MS_1 all goes through MS_4 instead of MS_3, and the start-up circuit is decoupled from the bias circuit.

4.3.6 Clock Generation

In the sample-and-hold circuit, clock signals are used to control the opening and closing of various switches. From Fig. 4.3, it is seen that sampling switches and input switches are closed on clock phase ϕ_1 while output switches are closed on clock phase ϕ_2; therefore, a two-phase complementary non-overlapping clock is needed.

On closer examination, it is found that the input switch should turn off slightly after the sampling switch turns off, otherwise it might lead to a loss of the signal being held. To see this, assume that the sampling switches and the input switches are controlled by the same clock signal. At the time the clock signal goes from high to low, the switches turns off. Due to the finite rise and fall time of the clock signal, the exact turn-off time of an MOS switch also depends on the threshold voltage V_T of the transistor and the signal level at the drain and source of the MOS switch. Therefore, it is possible that the input switch turns off before the sampling switch turns off. Later, when the sampling switch turns off, the input signal, which is a current signal, is absent from the input node and the signal being held on the hold capacitor is not the input signal at the end of the sampling mode. As a result, delayed clock signals have to be used. Also, the output switch should be turned on slightly after the sampling switch is turned off, therefore the two clock phases never overlap.

Fig. 4.7 shows a circuit used to generate complementary non-overlapping clock signals as well as the delayed version of the signal.

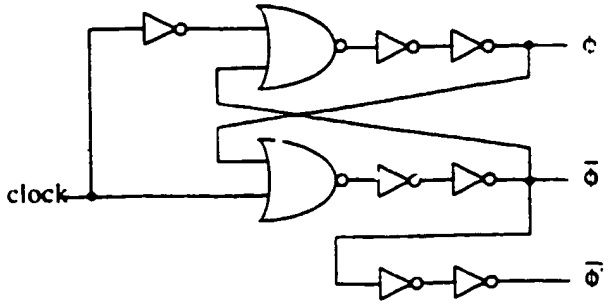


Figure 4.7 Clock generator

4.4 HSPICE Simulation

HSPICE simulation was used to verify the functionality of the circuit, to help choose component sizes, and to estimate the performance of the circuit. Both pre-layout and post-layout simulations were performed.

4.4.1 Component sizes

When choosing the component sizes, the bias currents are first set according to the constraint on power consumption of the circuit. For a power supply voltage of 3.3V, a current of 1.7 mA is chosen for the sample-and-hold circuit so that the power consumption of the circuit is about 5.5 mW. The bias circuit and common-mode feedback circuit consume very little power; therefore, the total power consumption of the circuit is less than 10 mW.

The sizes of the critical components in the sample-and-hold circuit are listed in Fig. 4.5. They are first chosen to ensure that the pole Q factor is less than $\frac{\sqrt{2}}{2}$ for the stability of the circuit. Refer back to Fig. 4.5, the bias currents I and J are set such that the transconductance g_m of the transistors Q_1 and Q_2 is larger than that of M_1 and M_2. The value of the hold capacitors C_{h1} and C_{h2} is set to be much larger than the value of C_π of the transistors Q_1 and Q_2. As a result the stability criterion can be easily achieved using Eq. (4.4). The sizes of M_1, M_2, C_{h1}, and C_{h2} are then adjusted for the desired small-signal 3-dB bandwidth. The sizes of the switches are decided for the required accuracy and sampling rate. The optimizations of the transistors' areas and geometries are done with HSPICE simulation. Remember that a trade-off between speed and accuracy exists, so these values are intended to deliver the best performance which meets the system specifications.

4.4.2 Simulation results

This section contains the HSPICE simulation results for the current mode sample-and-hold circuit. AC analysis is done to inspect the frequency response of the circuit. In particular, the small signal 3-dB bandwidth is examined. A DC sweep is carried out to find the maximum signal

swing. Fourier analysis gives the total harmonic distortion of the circuit, and the acquisition time was found with a transient analysis.

The DC sweep is run with input differential-signal of ±750 μA. The output signal-swing is found to be linear over the range of ±500 μA

Fig. 4.8 contains the waveforms from transient analysis when a full-scale pulse is applied at the input of the circuit. The graph contains the waveforms of the voltage signals held by the two hold-capacitors. From the simulation, it is found that the acquisition time of the circuit is around 5.6 ns, which implies a maximum clock frequency of 89 MHz.

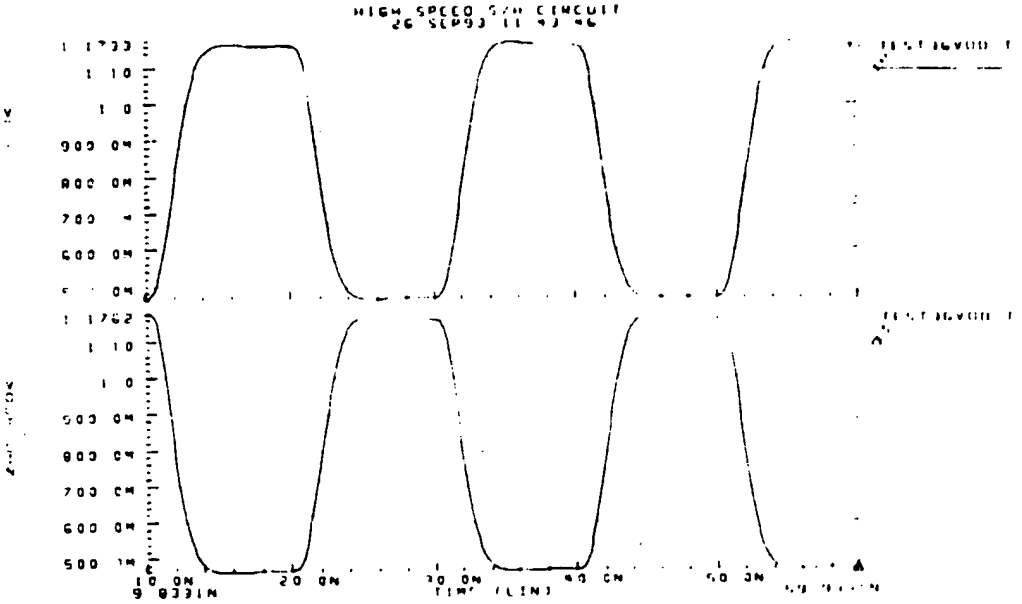


Figure 4.8 Transient analysis for the fully differential sample-and-hold circuit

The accuracy of the sampler is examined by checking the error signal between the input current signal and output signal held. Transient analysis is performed with constant input signals. At a sampling frequency of 83 MHz, for a differential input signal in the range of ±500 μA, the error-current is found to be around 0.102% of the signal current, which corresponds to an accuracy of 10 bits.

Fig. 4.9 contains the differential output signal of the sample-and-hold circuit when a 2MHz sine-wave input signal is sampled at a clock frequency of 50 MHz. The amplitude of the differential input current signal is 500 μA, and the output current signals are fed through 50Ω resistors.

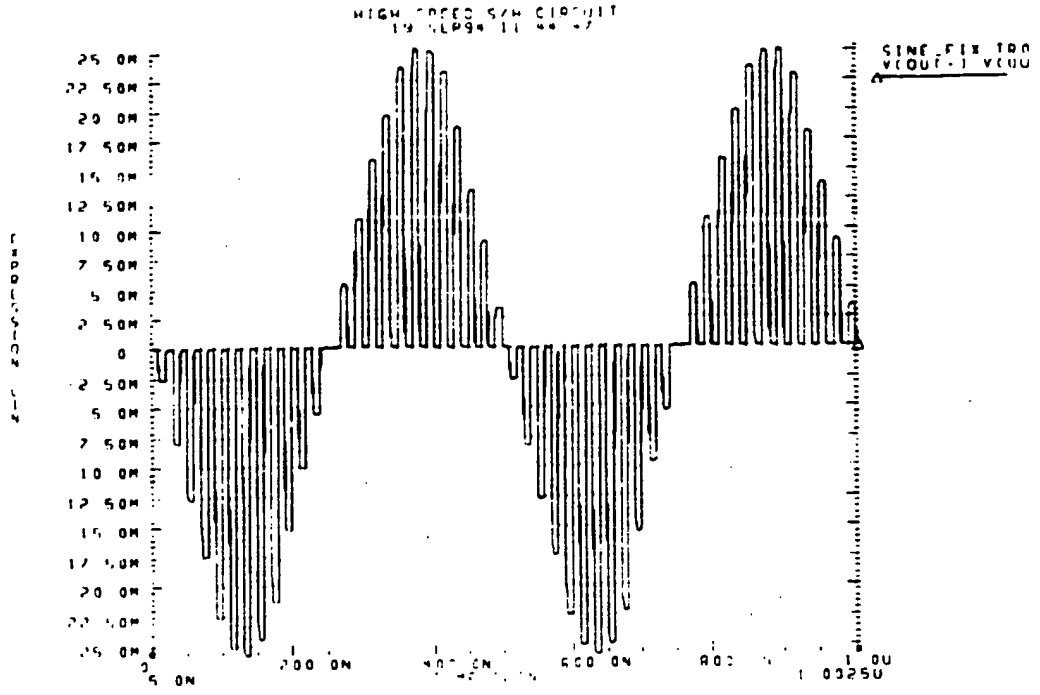


Figure 4.9 Output waveform of a 2MHz signal sampled at 50MHz

Fig.4.10 depicts the results from the AC analysis. From that, the input 3-dB bandwidth is found to be 155 MHz. As a comparison to the model derived earlier in this chapter, the calculated 3 dB bandwidth using Eq. (4.6) is 161 MHz. The difference is a result of the parasitics in the circuit, as well as the inaccuracy of the model.

The harmonic distortion was examined using the Fourier analysis in HSPICE. In HSPICE, Fourier analysis is performed on 101 points of transient analysis data on the last $\frac{1}{f}$ time period, where f is the fundamental Fourier frequency. The total-harmonic-distortion is calculated as the square root of the sum of the squares of the second through the ninth normalized harmonics. For a

Figure 4.10 AC analysis for the fully differential sample-and-hold circuit

fundamental Fourier frequency of 150.048 MHz. Fourier analysis shows a total harmonic distortion of 0.11%, in which the third-order harmonic is 0.08%.

Table 4.1 contains a summary of the simulation results for the current-mode sample-and-hold circuit.

Table 4.1 Summary of HSPICE simulation results for the sample-and-hold circuit

Power supply	3.3V
Power consumption	5.6 mW
Acquisition time	5.6 ns
Small signal 3dB bandwidth	155 MHz
Output signal swing	±500 μA
Accuracy	10 bits

4.5 Comparison with other Switched-Current Samplers

In this section, our sample-and-hold circuit is compared with two other types of switched-current samplers.

One type of switched-current sample-and-hold circuit is a two-step approach called S^2I

[34]. The circuit diagram and the clock waveforms are shown in Fig. 4.11. In that approach, high

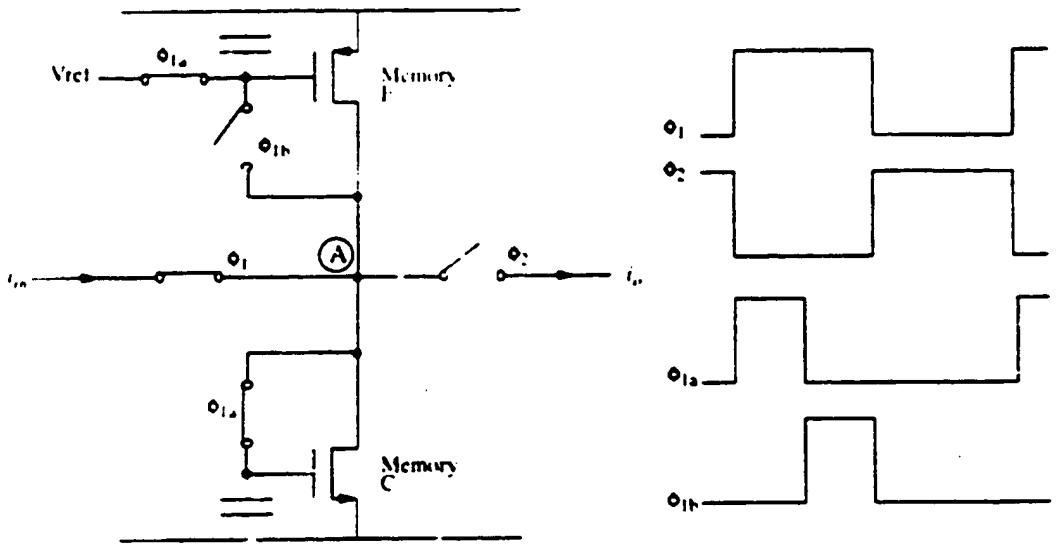


Figure 4.11 S^2I memory cell circuit and clock waveforms

accuracy is achieved by sampling the input current in a coarse step followed by a fine step. The signal sampled in the fine step is the error signal resulting from the charge injection from the coarse sampling, therefore it corrects the error in the output signal. The operation of the circuit can be explained briefly as follows. During phase ϕ_{1a}, the pmos Memory F is connected to V_{ref} and generates a bias current J. The current in the diode-connected nmos Memory C is $J + i_{in}$. At the end of phase ϕ_{1a}, the coarse memory switch is opened and the nmos transistor holds a current $J + i_{in} + \delta i$ where δi is the signal dependant error current resulting from charge-injection in the nmos. During phase ϕ_{1b}, the pmos is configured as a diode. With the signal current i_{in} still flowing at the cell's input, the pmos' drain current settles to the value $J + \delta i$. During phase ϕ_2, current $i_{in} + \Delta i$ is connected to the output, where Δi is the charge injection error in the fine memory resulting from the intermediate error δi, therefore it is much smaller. According to simulation [34], in a $0.8\mu m$ CMOS process, operating with a 5V power supply, the differential version of the circuit has a sampling frequency of 40 MHz and a transmission error of 0.07%

Observe that clock phase ϕ_1 is separated into ϕ_{1a} and ϕ_{1b} for the coarse and fine sampling. For a certain clock frequency, the switching of the switches controlled by ϕ_{1a} and ϕ_{1b} is twice as high as the clock frequency. This imposes an additional limit on the maximum sampling frequency achievable by the circuit. Another potential problem is that the input signal i_{in} might not be constant during phase ϕ_{1a} and ϕ_{1b}, and the difference of i_{in} from the end of ϕ_{1a} to the end of ϕ_{1b} will be sampled onto the fine memory, and this directly contributes to a signal dependent charge-injection error. In addition, there is glitching present in the output signal due to the fact that the internal node A of the circuit changes from a low impedance state to a high impedance state during the non-overlapping period of the clock [35], which of course is a problem for all types of switched-current sampler where a non-overlapping clock scheme is required.

Another type of switched-current sampler uses the zero-voltage switching technique proposed in [36]. The circuit diagram is shown in Fig. 4.12. In this design, the amplifier, A, and

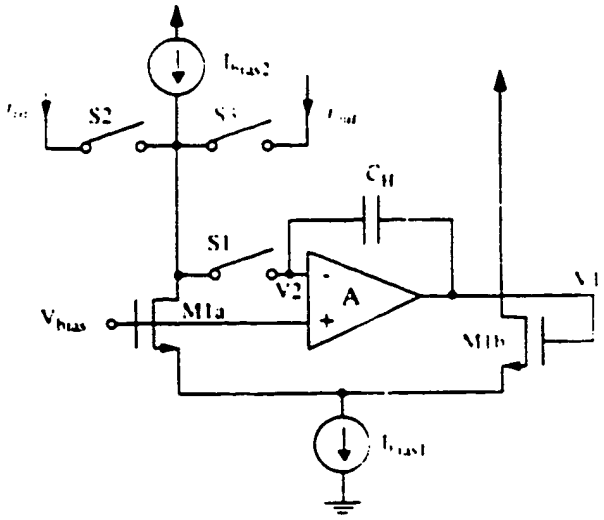


Figure 4.12 A zero-voltage SI current sampler

the hold capacitor, C_H, are used to sample the differential voltage required by M_{1a} and M_{1b} to make the current in M_{1a} $I_{in} + I_{bias2}$. The signal-dependant part of the charge injection error is largely eliminated because the negative feedback of amplifier A keeps the potential at the drain of M_{1a} constant. The remaining signal independent part of the charge injection can be eliminated by

extending the circuit into a fully-differential one. According to [36], the circuit was simulated in a 1.2μm CMOS process. With a power supply of 3.3V, the sampler achieves a maximum sampling frequency of 50 MHz and an accuracy of 14 bits.

By examining the circuit more closely, it is noticed that there are two stages in this circuit: the first stage of the differential pair M_{1a} and M_{1b}; and the second stage of the amplifier, which, most likely, consists of another differential pair. With the two-stage configuration, the speed of this circuit is limited compared to the switched-current sampler designed in this thesis where a common-base bipolar transistor was used to realize the amplifier and thus the circuit achieves speeds which are comparable to that of the basic sampler. Another fact that limits the speed of the zero-voltage switching current sampler is that, in order for this circuit to be stable, the transconductance g_{m1} of M_{1a} and M_{1b} must be smaller than the transconductance g_{m2} of the amplifier A. On the other hand, the bandwidth of the sampler tends to $\frac{g_{m1}}{C_H}$. As a result, the speed of the circuit is reduced from that achievable with other circuits [36].

The simulated performances of these two circuits and the circuit designed in this thesis are summarized in Table 4.2.

Table 4.2 Comparison of performance of different switched-current samplers

	Process	Sampling Rate	Accuracy
S^2I Memory Cell	0.8μm CMOS	40 MHz	> 10 bits
Zero Voltage SI Sampler	1.2μm CMOS	50 MHz	14 bits
Our SI Sampler	0.8μm BiCMOS	89 MHz	10 bits

From the comparison, the conclusion can be drawn that the switched-current sampler designed in this thesis takes advantage of the speed of bipolar devices, and therefore it has the highest sampling rate. However, both the zero-voltage switching SI sampler and the S^2I memory cell exhibit greater accuracy since the signal-dependant part of the charge-injection error is reduced. Although the zero-voltage switching SI sampler exhibits a higher resolution compared to

the S^2I memory cell, an amplifier is required, therefore the circuit is more complicated.

4.6 Summary

This chapter discussed the design issues of the switched-current sample-and-hold circuit. Since a trade-off between speed and accuracy exists, efforts were made to optimize the circuit performance and to meet the specifications for the circuit. The design was compared with two other switched-current samplers to highlight the strengths and weaknesses of the circuit. In the next chapter, layout and implementation of the sample-and-hold circuit are discussed. Testing of the sample-and-hold circuit and the results are also presented.

CHAPTER 5 Implementation and Testing

5.1 Layout

Layout has a great impact on circuit performance in analog circuit design. In general, the performance and function of an analog circuit depends heavily on the precision of its components. The parasitics associated with device placement and routing are unavoidable and thus it is hard to keep component values precise. As a result, analog circuits are more sensitive to layout induced performance degradation than digital circuits.

For the design in this work, a 0.8μm BiCMOS process is used for chip fabrication. Mentor Graphics' GDT is used as the layout tool, and hierarchical, parameterized functional blocks are written for flexibility and easy modification of the layout.

Layout effects can be grouped roughly into three categories: circuit loading effects, signal-coupling effects, and matching deficiencies effects [37]. To reduce loading effects, which result from capacitive and resistive circuit elements introduced by inter-device wiring, and are associated with the geometry of the devices themselves, the parasitics resulting from inter-device wiring must be reduced. To achieve this, critical wires are made as short as possible by placing connected devices in close proximity. For MOS circuits, the dominant layout capacitance is

associated with the gate structure. The gate capacitance itself is fixed since the gate area is fixed for a given design. However, the non-linear voltage-dependent junction capacitance at source and drain regions can be reduced by minimizing the size of all diffusions. In this design, device folding is used for large-size MOS devices (current sources) to allow a single source or drain diffusion to be shared by two gate regions. Furthermore, device merging is used to place electrically connected devices in such a way that diffusion geometry is shared between them. This kind of geometry-sharing has the additional advantage of improved packing density.

Unexpected signal-coupling can also be introduced into a circuit during layout which may inject unwanted electrical noise or even destroy the stability of the circuit through unintended feedback. Two conductors can have a capacitive coupling if they are on different layers and they cross, or if they are on the same or different layers and they run adjacently. The coupling capacitance is proportional to the area of the crossing or to the length of the adjacent run, respectively. In this design, the crossing or parallel running of incompatible signals are minimized in order to reduce these couplings. The complementary clock signals are run in parallel, and a ground line is put between the two clock signals to act as a coupling shield.

Resistively coupled signals are particularly troublesome in power supply lines. They are reduced by decreasing the resistance of power supply lines through reducing their length and increasing their width. Power line noise is reduced by connecting a large capacitor from V_{dd} to ground. In order not to consume too much area from the layout, the gate capacitance of an MOS transistor is used. The source and drain of the transistor are tied together and connected to power line V_{dd}, while the gate of the transistor is connected to the ground line. This large MOS transistor is laid out underneath the V_{dd} line, therefore it does not itself occupy any additional area.

Signals can also be coupled through the silicon substrate. Since all devices share the same substrate, noise injected into the substrate is capacitively or resistively coupled into every node of the circuit. Substrate coupling is minimized by liberal placement of substrate contacts which

reduce noise by shunting stray currents out of bulk. This also helps to reduce the danger of latch-up.

Matching effects include both device matching and parasitic matching. Variations are unavoidable in all processes, and they lead to small mismatches between supposedly identical devices. When the mismatch is large enough, it can affect circuit performance. For the fully-differential circuit in this design, good matching between components is especially important. To improve matching of identical devices, they are created using identical geometries thus subjecting them to the same geometric distortions. The largest possible size is used for matched devices since mismatch tends to decrease with increasing device size; they are placed in the same orientation since many processing effects introduce anisotropic geometric differences. Also they are placed in close proximity or spacially interdigitated in an attempt to cancel out the effects of global process gradients.

In this fully-differential circuit, capacitive and resistive components are matched by using mirror-symmetry, in which the placement and wiring of matching circuits are forced to be mirror-identical. The absolute values of the hold capacitors are less important than their ratio, therefore, a unit cell approach is employed when laying them out.

Fig. 5.1 contains a layout plot of the circuit. This layout diagram contains a limiting amplifier, which occupies the lower portion of the layout, and the sample-and-hold circuit designed in this thesis. For the sample-and-hold circuit, the bias circuit is laid out at the bottom of the diagram. The middle part contains the P-channel sources. The main circuit, which includes the MOS sampling devices, capacitors, and the switches, is shown in the upper portion of the plot. Some pads were added in the layout for checking the bias points. The two hold-capacitor nodes were connected to the output pads so that functionality of the circuit could be checked.

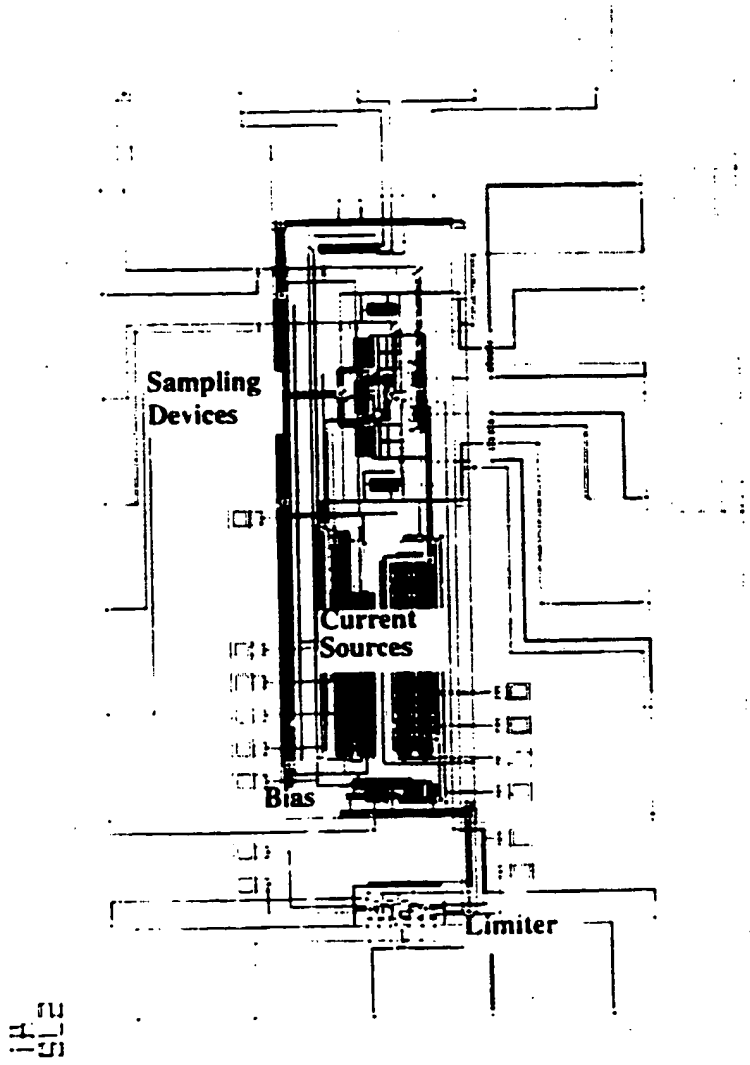


Figure 5.1 Layout diagram of the sample-and-hold circuit

5.2 Fabrication and Packaging

The sample-and-hold circuit is fabricated using Northern Telecom's 0.8μm BiCMOS process with three layers of polysilicon and three layers of metal [38].

Packaging is a major concern due to the fact that bondwires, lead inductances, and pin-to-pin capacitances from packaging degrade the performance of the circuit. For this circuit, the LCC 44-pin package is used.

5.3 Testing Setup

The circuit diagram of the fully-differential sample-and-hold circuit designed can be found in Fig. 4.5.

The input signal required for the sample-and-hold circuit is a differential current signal. However, the signal from the function generator is a single-ended voltage signal. Therefore a single-ended to differential transformer is used to convert the single-ended voltage signal to a differential voltage signal. In order to supply a current signal to the input, a voltage-to-current converter is used to convert the voltage signal to a current signal. In this case, a resistor is used as a simple voltage-to-current converter. Notice that the sample-and-hold circuit designed has a low input impedance, therefore there is no need to use a resistor with very large value for converting the voltage to current. In this setup, a resistor of $4k\Omega$ is used. In front of the voltage-to-current conversion resistor, an off-chip 50Ω resistor is used for impedance matching with the shielded 50Ω coaxial cable. The signal from the function generator is then AC-coupled into the circuit. The circuit diagram for the generation of the input signal is illustrated in Fig. 5.2.

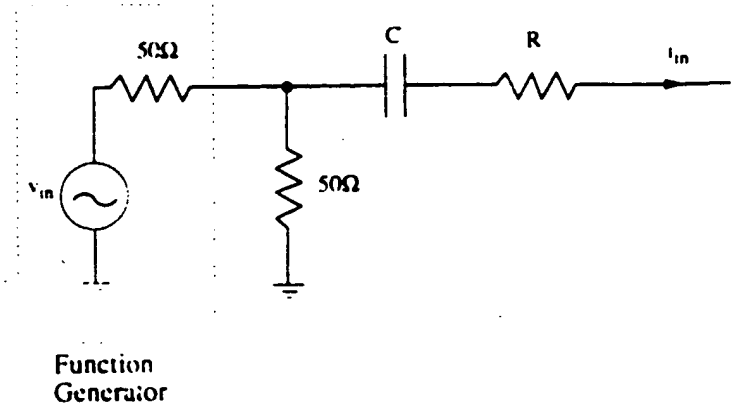


Figure 5.2 Generation of input current signal

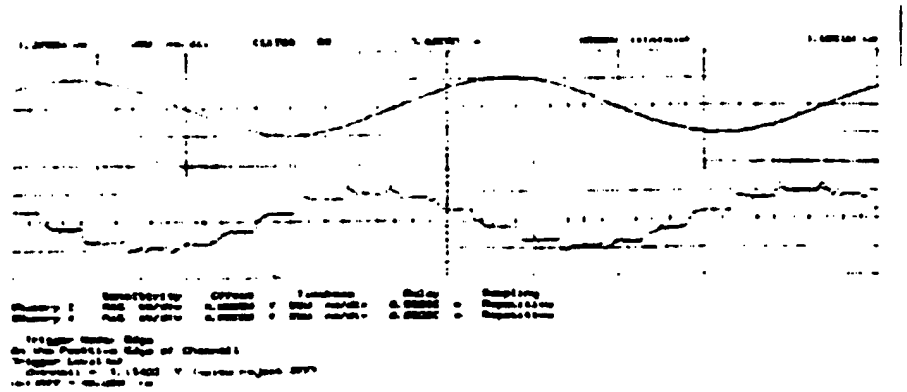
To check the accuracy and speed of the circuit, the output current signal of the circuit is examined. Resistors are used to convert the current signals into voltage signals. The differential output signals are then summed up into a single-ended signal using a differential to single-ended transformer, which is simply the reverse of the single-ended to differential transformer used at the input of the circuit.

5.4 Functionality Testing

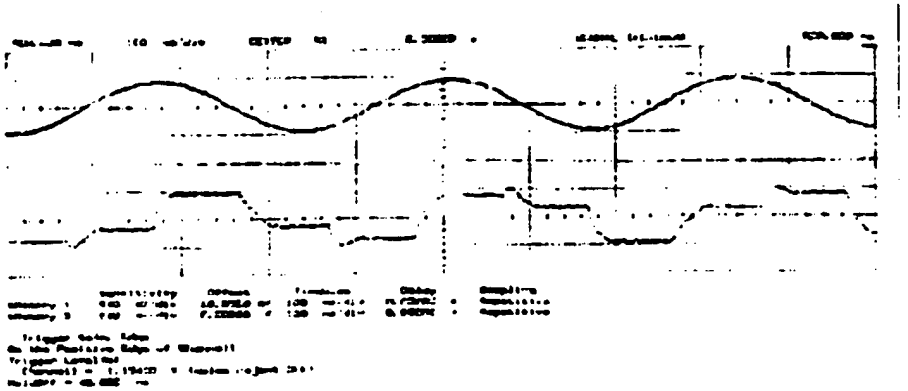
The functionality of the circuit was first verified at low frequencies. A Wavetek 395 function generator was used to generate the input signals, and the signals at the hold capacitance nodes were examined. The signals were displayed on the HP54501 Digitizing Oscilloscope using $1M\Omega$ high-impedance probes. Fig. 5.3 contains the plots of the input and the output signals at the hold-capacitor nodes.

The accuracy of the sampler is examined by applying a square wave input signal, and checking the output signal value during the hold mode for the error current. For a clock signal of 10 MHz, and the differential input signal in the range of ±500 μA, the error signal is found to be 0.08% which corresponds to an accuracy of 10 bits.

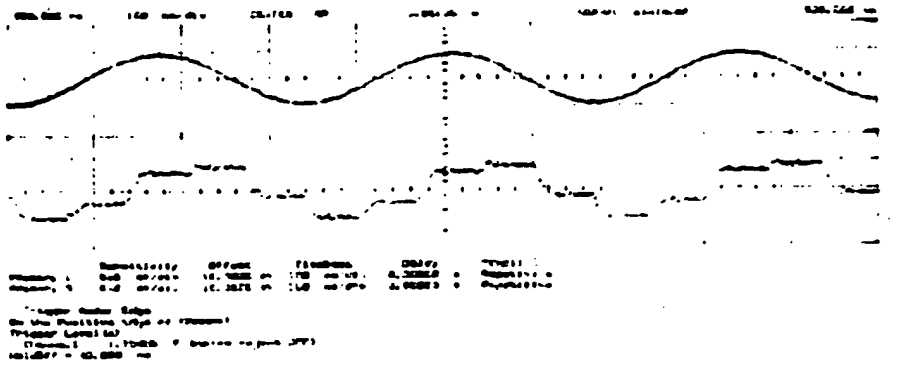
The functionality of the sample-and-hold circuit as a decimator is also verified. For this purpose, a sinusoidal input signal of 10 MHz is applied to the circuit. A square wave signal of 2.51 MHz is used as the clock. The output of the circuit is fed into the HP 3588A Spectrum Analyzer. An LM592 differential video amplifier is used to increase the signal strength at the output of the sample-and-hold circuit before the signal is connected to the spectrum analyzer. According to the sampling theorem, the spectrum of the sampled signal should contain components at frequencies $(10 \pm n \times 2.51)$ MHz, where n is an integer. On the spectrum analyzer, the baseband signal at 40 kHz is observed. The second frequency component at 2.47 MHz, the third tone at 2.55 MHz, and higher frequency components are also found on the analyzer. The signal strength corresponding to various tones rolls off according to a sinc function.



(a)



(b)



(c)

Figure 5.3 Output waveforms: (a) f_{sig} = 1MHz, f_{clk} = 10MHz; (b) f_{sig} = 3MHz, f_{clk} = 10MHz; (c) f_{sig} = 3MHz, f_{clk} = 15MHz.

5.5 Performance of the Circuit

To characterize a sample-and-hold circuit, the two most important measurements are maximum clock rate and accuracy.

To measure the maximum clock rate, one way is to find the acquisition time of the sample-and-hold circuit by applying a full-scale signal at the input, and checking the rise time at the hold capacitance nodes. However, with the $1M\Omega/7pF$ probes, the capacitance at the hold capacitance nodes will become $7.65pF$ instead of the design value of $0.65pF$, and this will result in a much slower rise time.

An alternative is to measure the accuracy of the circuit at a moderate frequency, and then increase the clock frequency until the accuracy starts to decrease. The sampling interval corresponding to that clock frequency is taken as the acquisition time.

A Colby Instruments Inc.'s 3000A pulse generator is used to provide the differential clock signals at high frequencies. The output of the sample-and-hold circuit is amplified with the LM592 differential video amplifier and is then sent into the spectrum analyzer where harmonic distortion was observed. From the functionality testing, the accuracy of the sample-and-hold

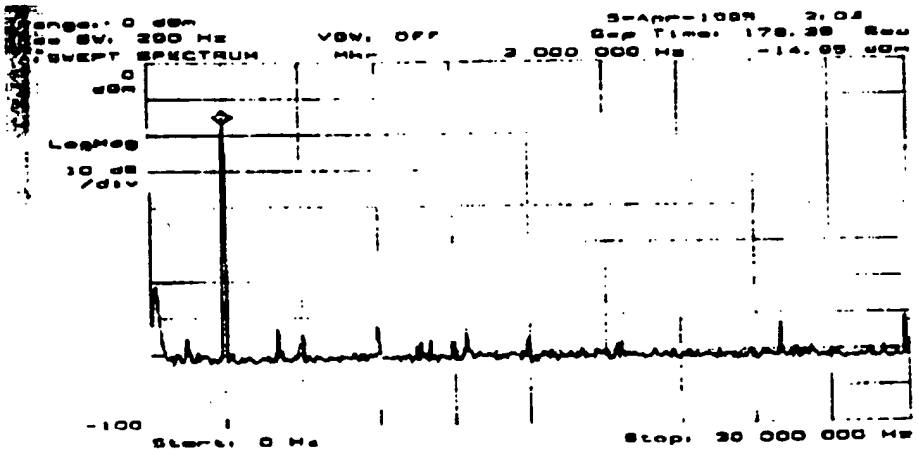


Figure 5.4 Output spectrum: f_{sig} = 3MHz, f_{clk} = 57MHz

circuit is found to be 10 bits. To maintain this accuracy, it is found that the maximum clock frequency achievable is 57 MHz. In Fig. 5.4, a plot from the spectrum analyzer with an input signal at 3 MHz and a clock signal at 57 MHz is shown.

5.6 Testing Results and Discussion

In Table 5.1, the performance of the sample-and-hold circuit is summarized.

Table 5.1 Summary of the performance of the sample-and-hold circuit

Process	0.8μm BiCMOS	
Circuit Area	0.26 mm^2	
Power Consumption	Supply Voltage	3.3 V
	Supply Current	1.8 mA
	Power Consumption	5.94 mW
Performance	Sampling Frequency	57 MHz
	Differential Signal Swing	±500 µA
	Total Harmonic Distortion	- 60.43 dB
	Linearity	10 bits
	CMRR (sample-mode)	53 dB
	Power Supply Range	2.8 - 4.5 V

The measured results match the simulation results (Table 4.1) quite well except for the maximum sampling rate. The reason for this degradation is that in the layout, the two hold capacitance nodes were connected to the output pads so that they could be accessed during testing to check the functionality. Extra capacitance is added on top of the $0.65pF$ hold capacitors. By checking the process, an extra capacitance of $0.5pF$ was estimated for the output pads. Re-simulating the circuit in HSPICE with additional capacitance, the acquisition time is 8.2 ns which corresponds to a maximum sampling rate of 61 MHz. Notice also that the two capacitance nodes need not to be accessed when the sample-and-hold circuit is used. Therefore, the conclusion can be drawn that a sampling rate of more than 80 MHz is feasible.

CHAPTER 6 Conclusion

6.1 Conclusion

In this thesis, a sample-and-hold circuit was designed. First, various architectures for sample-and-hold circuits were studied and compared. The switched-current technique was selected due to its low-voltage operation and simple circuits which result in a low power consumption. During the design of the circuit, effort was made to achieve a high sampling rate and high accuracy, while controlling power consumption. The circuit was then fabricated in Northern Telecom's 0.8µm BiCMOS process. Experimental testing was done to show that the switched-current sampler exhibits an accuracy of 10 bits at a sampling frequency of 57 MHz. The testing and simulation results also suggests that for this circuit, sampling frequencies beyond 80 MHz are feasible.

One application of the sample-and-hold circuit is in the receiver of the CT2Plus wireless communication system. The functionality of the sampler as a decimator was verified. Experimental results also show that the sample-and-hold circuit can operate with the supply voltage ranging from 2.8V to 4.5V. The power consumption of the circuit is 5.94 mW at 3.3V voltage supply. The low supply voltage operation and low power consumption make it suitable for

wireless system applications.

6.2 Suggestions for Future Work

For the sample-and-hold circuit designed in this thesis, dummy switches were used to reduce the charge injection errors. In this design, the widths of the dummy switches were half of that of the switch transistor. However, for maximum charge-injection cancellation, the width of the dummy switch should be larger than half of the width of the switch transistor. Although it is difficult to derive the size of the dummy switch analytically, HSpice simulation can be used to help finding the appropriate size. This can result in a higher accuracy for the sampler without sacrificing the operational speed of the circuit.

To solve the problem of reduced maximum sampling rate, current mirrors can be used to provide the signal functionality testing. This eliminates the need to probe the hold-capacitance nodes.

The application of this sample-and-hold circuit is in the receiver of the CT2Plus personal communication radio. From Chapter 2, it is indicated that two major blocks in the receiver system are a sample-and-hold circuit and a limiting amplifier. Due to the fact that the sample-and-hold circuit designed in this thesis is a current-mode circuit, in order not to add extra complexity of designing voltage-to-current converter and current-to-voltage converter between the circuits, it is more appropriate to have the limiting amplifier designed to have a current output.

One possible starting point is that a simple differential pair, as the one shown in Fig. 6.1,

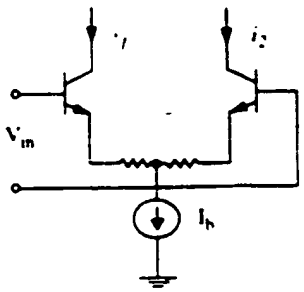


Figure 6.1 A differential pair as a current limiter

can act as a current limiter. However, in order to connect the output currents i_1 and i_2 to the input of the sample-and-hold circuit, appropriate voltage levels at the output of the current limiter need to be considered.

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